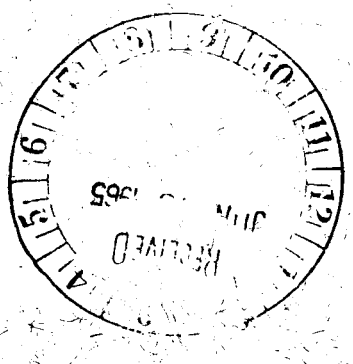
S-782

DESIGN, DEVELOPMENT, FABRICATION, AND DELIVERY OF THREE (3) STRAIN GAGE ACCELEROMETERS

Contract No. NAS8 11633

Final Report

June 23, 1964 - June 23, 1965



NASA

George C. Marshall Space Flight Center
Huntsville, Alabama

Prepared by

RAYTHEON COMPANY
Research Division
Waltham, Massachusetts 02154

DESIGN, DEVELOPMENT, FABRICATION, AND DELIVERY OF THREE (3) STRAIN GAGE ACCELEROMETERS

Contract No. NAS8 11633

Final Report

June 23, 1964 - June 23, 1965

NASA

George C. Marshall Space Flight Center
Huntsville, Alabama

Prepared by

RAYTHEON COMPANY

Research Division

Waltham, Massachusetts 02154

G. Doering
W. Rindner
R. Wonson

FOREWORD

This report was prepared by Raytheon Company, Research Division, Waltham, Massachusetts under Contract No. NAS8 11633, with Mr. Alonzo Davis acting as project engineer. This report covers work conducted from June 1964 to June 1965.

ABSTRACT

A program of research and development was performed with the object of providing dc accelerometers based on the anisotropic stress effect in p-n junctions. Initial difficulties in fabrication of piezojunction devices were overcome during this program. Piezotransistors, stress-sensitive integrated circuits, and acceleration sensors based on each were assembled and evaluated. The best sensors exhibited sensitivities exceeding 100 pk mV/pk G, frequency response within 5 percent from dc to 5000 Hz, linearity better than 5 percent over a 40 dB range, and a weight of 0.5 gram. Thermal zero shift of 1 percent FS/F° and sensitivity shift of 0.1 percent FS/F° were demonstrated, and feasibility was shown of a method to compensate the excessive drift. Efforts to encase sensors in protective housing failed, but not because of any basic limitation.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd.)

1. INTRODUCTION

1.1 The Anisotropic Stress Effect in P-N Junctions

For the past few years, transducers, unlike many other electronic components, have not shared the rapid advance towards microminiature size. An effect discovered in Raytheon's Research Division in 1961, the anisotropic stress effect (ASE) in semiconductor junctions,[1,2] had opened a new potential for miniaturization and integration of a wide range of electro-mechanical transducers in microcircuits. Laboratory samples of devices making use of the ASE were being studied at the time work began on this contract.

The ASE basically manifests itself as a very large and reversible resistance change - by factors up to several orders of magnitude - of a p-n junction when it is subjected to appropriate stresses. The characteristic features of the effect are that the stress be anisotropic and that the local stress magnitude be very high (10^9 to 10^{10} dyn cm^{-2}). The latter condition is easily fulfilled with small applied forces in view of the necessary anisotropy of the stress. The advantages offered by modern semiconductor devices make the ASE a particularly attractive mechanism for new transducers, which we refer to generically as piezo-junction (P-J) devices.

The effect was first observed under the mechanical conditions diagrammatically represented in Fig. 1. A diamond stylus (such as those used in phonograph pick-ups) is pressed against the semiconductor surface parallel to the junction plane with forces of a few grams. The junction depth has to be of the order of 1μ, or preferably less. Depending on the magnitude of the stresses applied and on the junction used, reproducible changes in both the reverse and forward bias resistance are obtained; the resistance changes reach several orders of magnitude under proper conditions. Figure 2 illustrates the character and magnitude of these stress-induced resistance changes in a germanium diode. Particularly

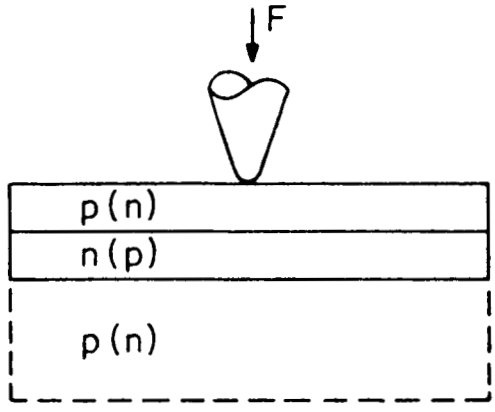
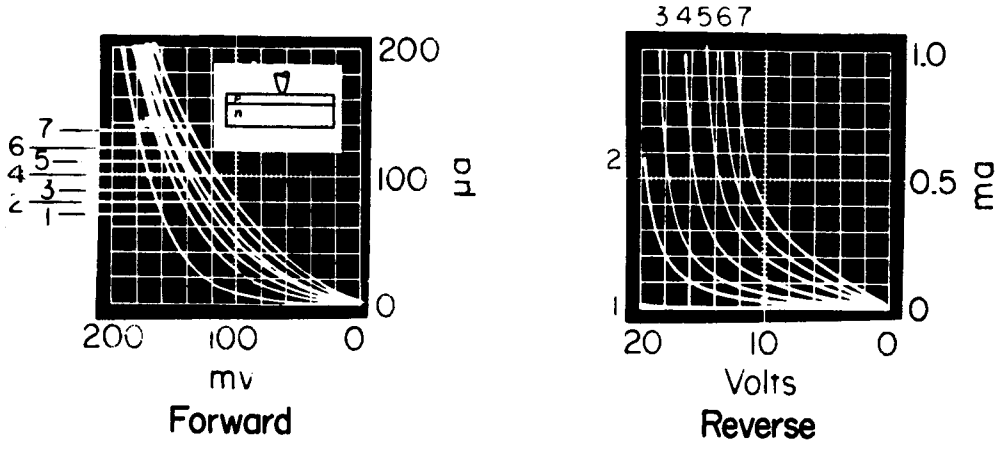


Figure 1 Schematic of Experimental Conditions For the ASE. The Junction Stressed Can Be Any One in a Multi-Layer Structure



1) No stress 2) 2000 dynes 3) 2250 dynes 4) 2500 dynes
5) 2750 dynes 6) 3000 dynes 7) 3250 dynes

Figure 2 The ASE in a Germanium Diode

striking is the effect under reverse bias where the breakdown characteristic is strongly affected. In silicon the effect is qualitatively very similar to that in germanium but generally somewhat smaller in magnitude.

Obviously, if stress can affect the characteristics of a single junction this dramatically, it can be expected to affect as strongly the characteristics of any multi-junction device with one junction subjected to the stress. The most prominent multi-junction device is, of course, the transistor, and indeed, from a practical point of view, in this device are found the most interesting manifestations of the ASE. Stress applied to the emitter-base junction generally reduces the current gain of the transistor by as much as three orders of magnitude (Fig. 3).

In view of the nature of the phenomenon, the list of manifestations of the ASE is at least as extensive as that of existing multi-junction devices, and little purpose would be served in continuing it. Suffice it to mention as additional examples the ASE in negative resistance devices such as the avalanche transistor and the tunnel diode. The avalanche transistor deserves particular mention because, by its peculiar response to stress - a change in its breakdown characteristics, analog-to-digital conversion in integrated piezo-junction transducers was achieved in 1963. The tunnel diode on the other hand (its characteristics under stress are illustrated in Fig. 4) has played a significant role in elucidating the physical origins of the ASE. [3]

1.2 The Basic Piezo-Junction Element

The problem of harnessing the effect to perform practical transducing functions is quite formidable, as can be readily visualized considering the minute dimensions involved. Some of the difficulties that must be overcome with our stressing arrangement are quite evident: the stylus must have minimum constraint along its axis; there must be no sliding along the semiconductor surface; and provision must be made for a stress bias. Shortly before work began on this contract, we had reduced to practice a basic

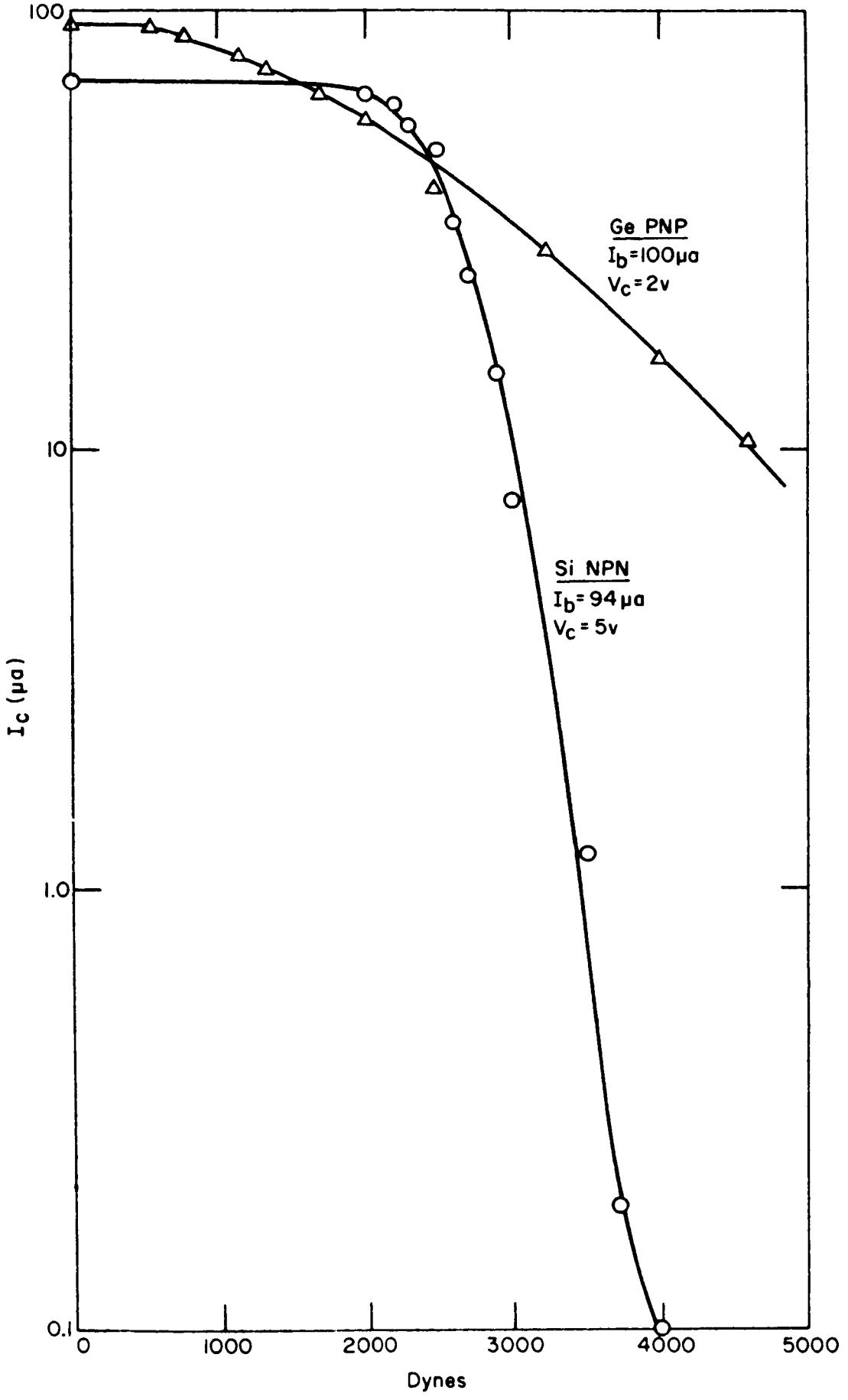


Figure 3 The Effect of Anisotropic Stress on the Current Gain of Two Transistors

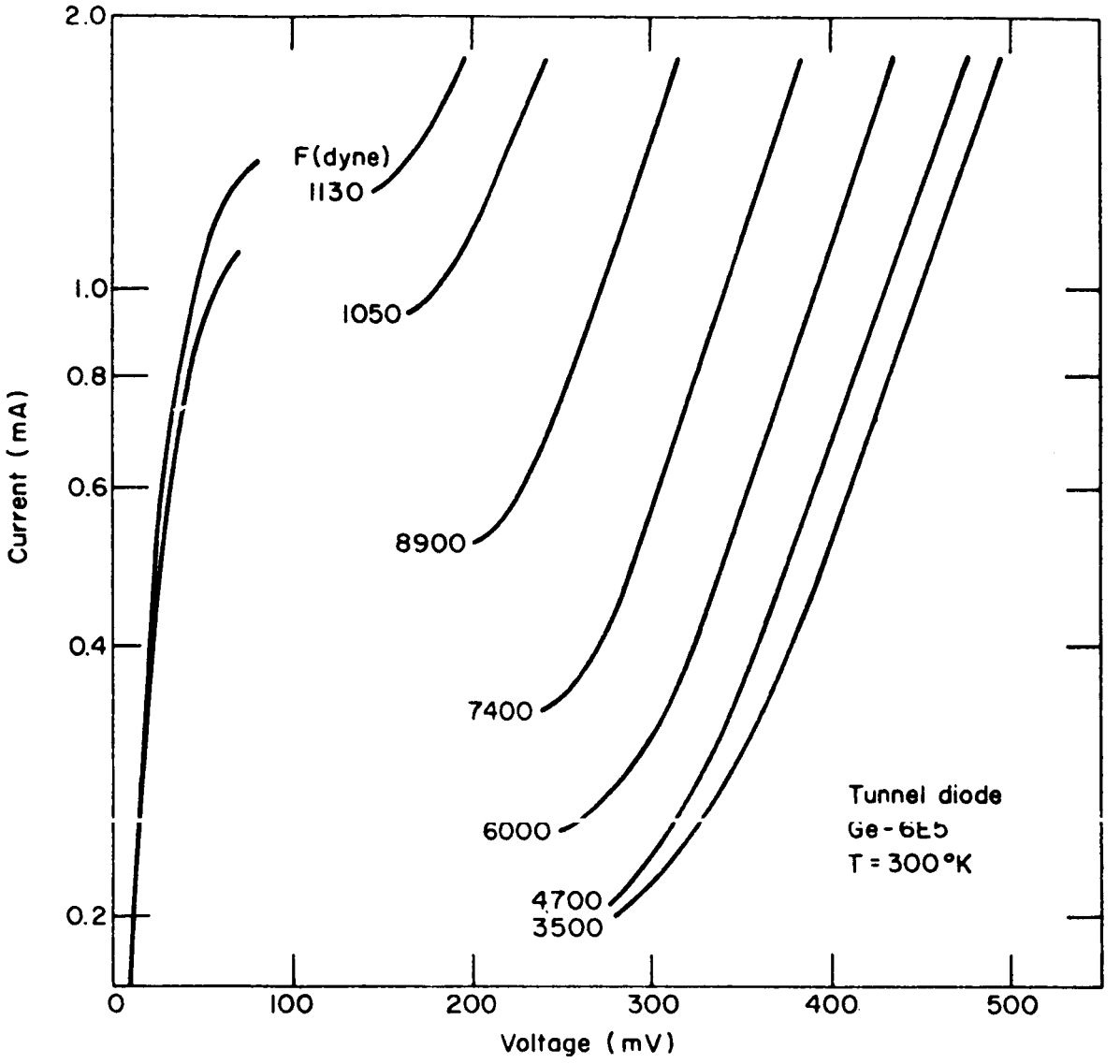


Figure 4 The ASE in a Germanium Tunnel Diode

sensor designed to serve as the core of various transducer applications. The object was to integrate the stylus and transistor chip into an easily handled, self-contained package, which the transducer designer could utilize merely by providing a means of holding the package and introducing the appropriate force to be transduced. Figure 5 shows in schematic form the steps in the assembly of such a device. The resulting structure - our basic element - looks exactly like a conventional transistor. Because of the small masses involved, the element withstands considerable shock - for example, it can be dropped without showing evidence of damage. On the other hand, stroking with a small artist's brush produces output signals of several volts.

1.3 Early Applications

1.3.1 Accelerometer

The basic element was designed to be usable in a variety of structures, according to the device function desired. In particular, we had incorporated the basic element in an accelerometer shown in cross section in Fig. 6. The seismic mass is attached by epoxy bonds to the center of the membrane of the basic element and to a second parallel steel membrane welded to the rim of the subassembly. The total weight of the device was about one gram. The initial evaluation of such an accelerometer yielded the following results:

The sensitivities ranged from 6.4 pk mV/pk g to 22.6 pk mV/pk g, depending on the bias chosen. The signal/noise ratio was largely independent of bias, a typical noise level being approximately equivalent to 0.05 g acceleration.

The linearity over a dynamic range exceeding 40 db (0.3 g to 56 g) was within 1 db of the best straight line for all points, as shown in Fig. 7, for two different arbitrary bias conditions.

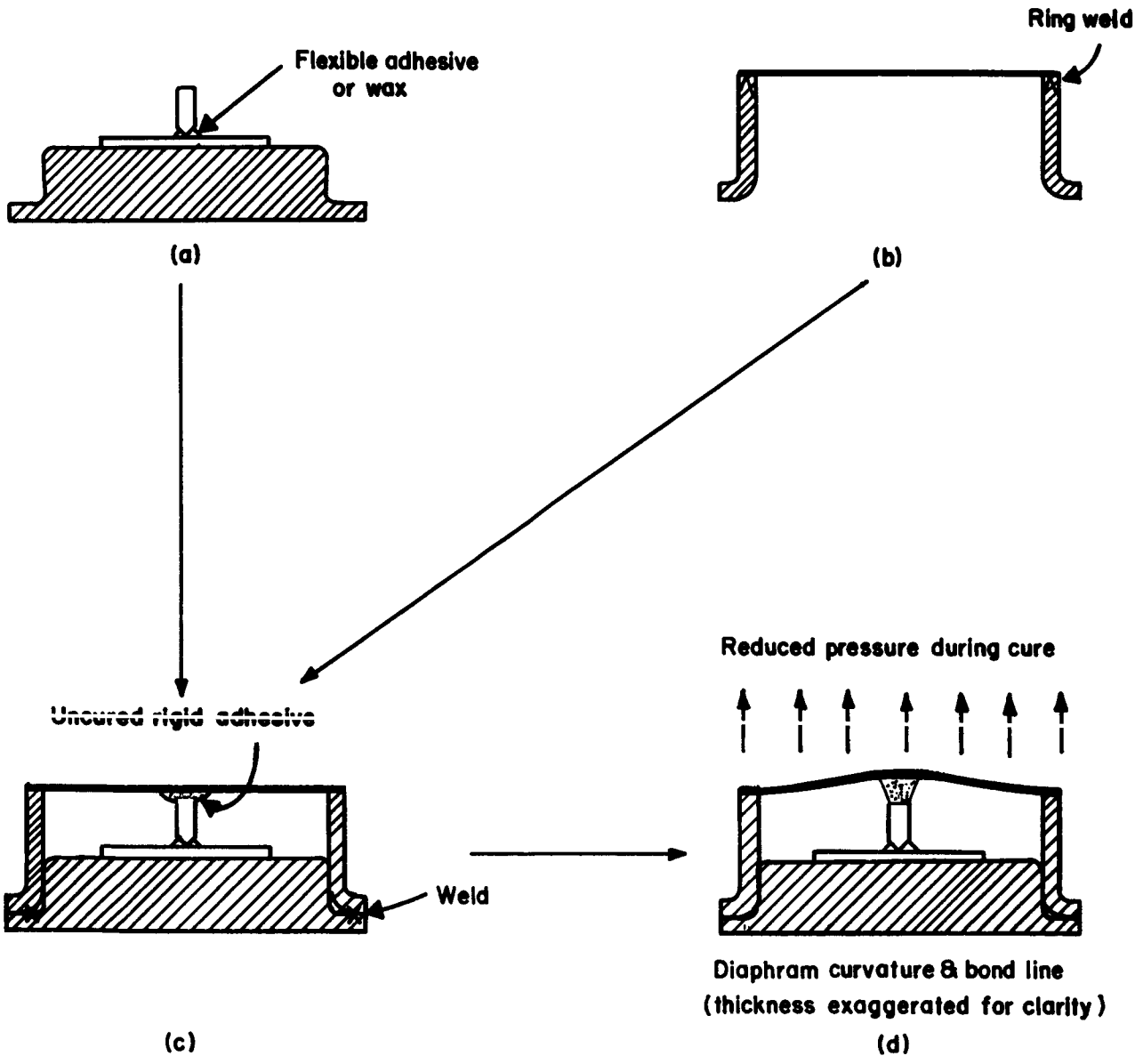


Figure 5 Successive Stages in the Assembly of Piezo-Transistors

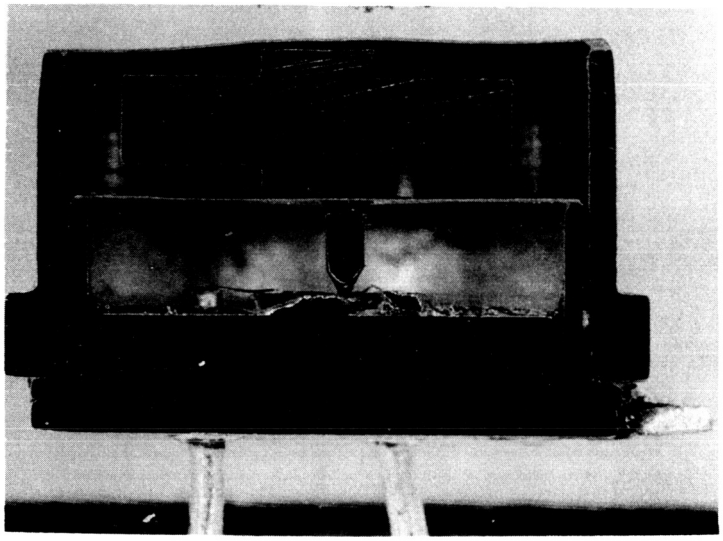


Figure 6 Cross-Section of a Piezo-Transistor Accelerometer

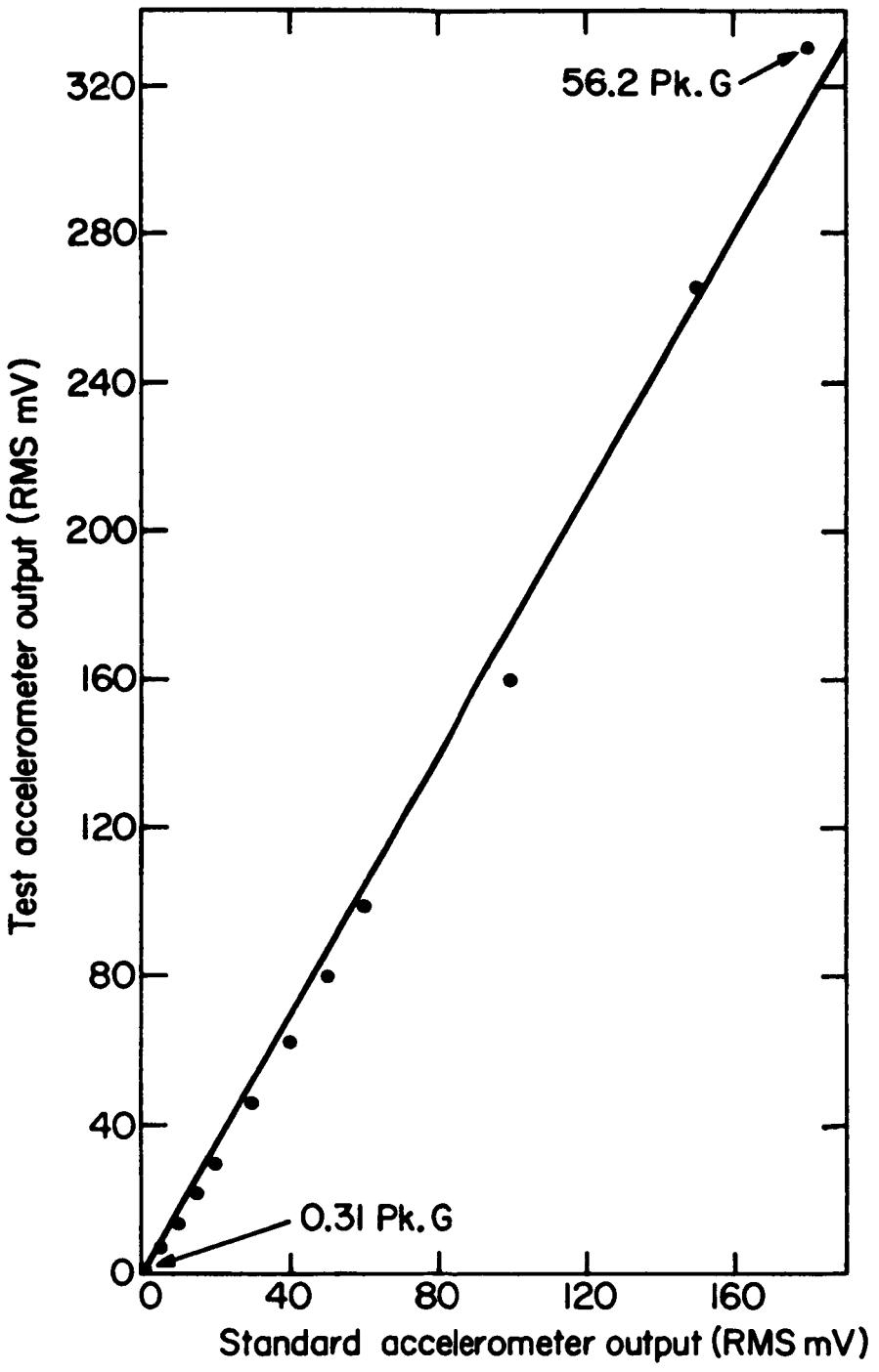


Figure 7 Output of a Piezo-Transistor Accelerometer Referred to the Output of a Standard Accelerometer

Frequency response, which extends to dc (Fig. 8), was measured over a range from 20 cps to 20 kc and found to be flat within ± 1 db up to 7200 cps. Phase shift was negligible up to 8 kc. The resonance occurred at about 15 kc.

1.3.2 Phonograph Pickup

A few simple processing steps converted the basic piezo-transistor to a phonograph pickup with surprisingly good tonal quality, considering the unsophisticated design. Figure 9 shows such a pickup which comprises the basic piezo-transistor and a pliable needle attached to the membrane by an epoxy bond and terminating in a diamond point. The needle, lying in the plane of the membrane, transfers practically none of the pickup weight to the transistor but is sufficiently effective in converting the lateral signals from a record into electrical output. Figure 10 shows a typical frequency response curve of such a pickup as well as, for comparison, the response taken on the same test record of a conventional magnetic pickup in the same tone arm.

1.3.3 Avalanche-Mode Direct FM Devices

Having made some progress with the problems of putting the ASE to use in diodes and transistors, we also investigated the possibility of integrating the sensing element with its associated circuitry (under USAF contract) and of translating the stress input into digital output. The basis for this attempt was obvious: we were using essentially standard transistors or diodes as sensors, and thus the transducers are inherently compatible with transistor circuitry in all significant parameters such as impedance level, power supply requirements, etc. The basic idea was to use an oscillator circuit of some kind which would incorporate a stress-sensitive junction. We would then modulate the frequency of this oscillator by a stress input. The number of pulses per second could then, by standard techniques, be used as a digital measure of the stress input.

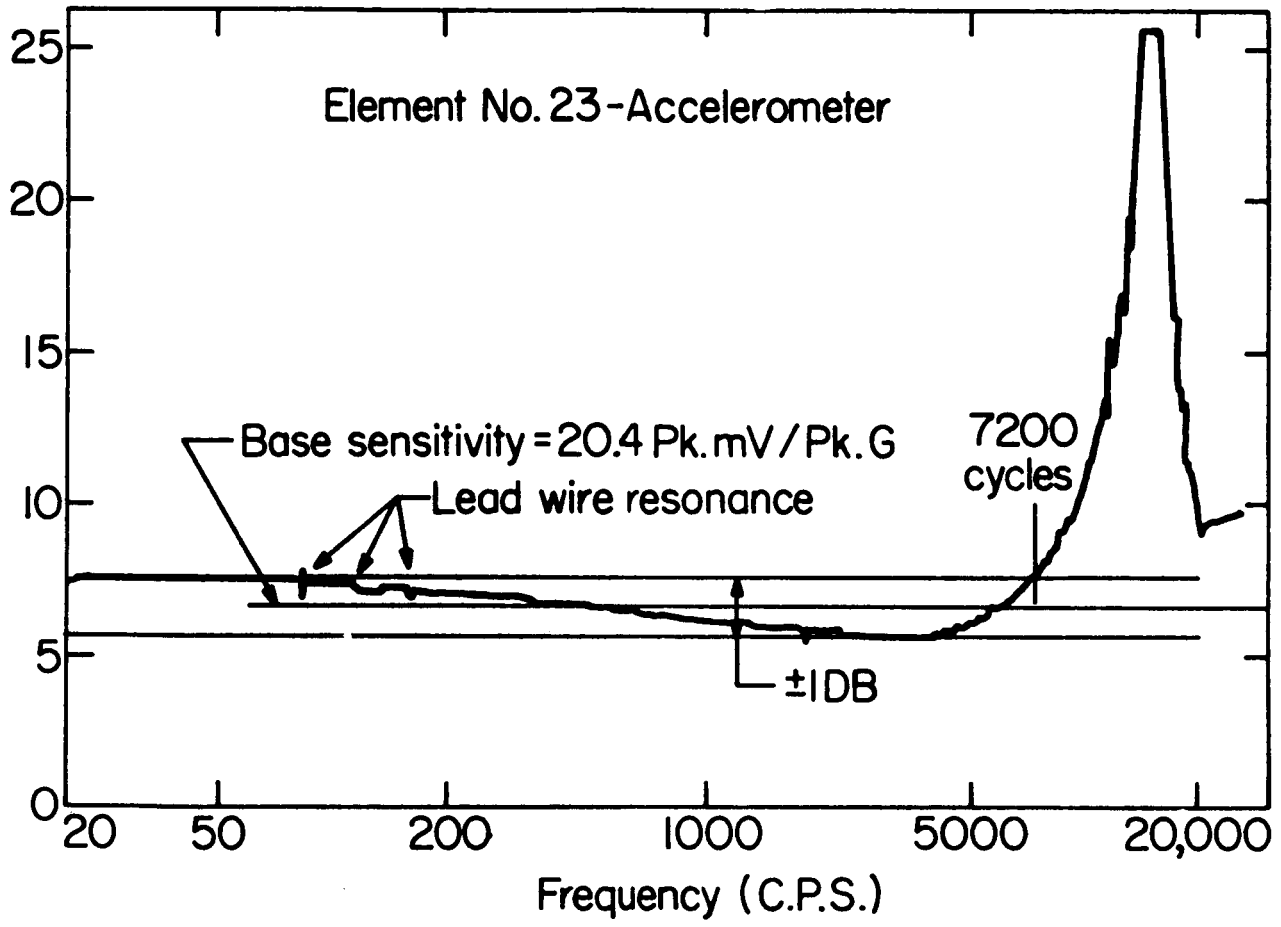


Figure 8 Frequency Response of a Piezo-Transistor Accelerometer

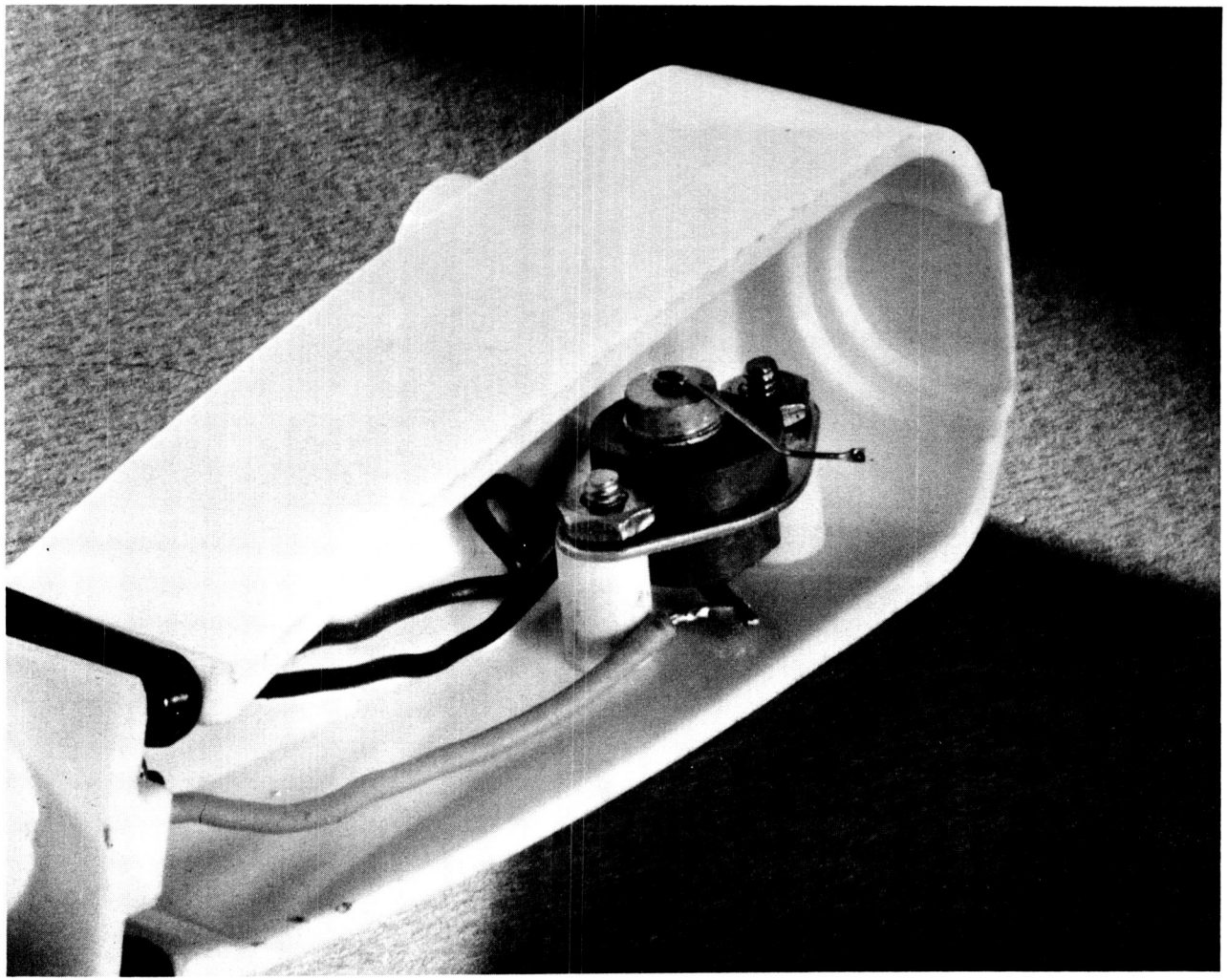


Figure 9 A Piezo-Transistor Phonograph Pickup

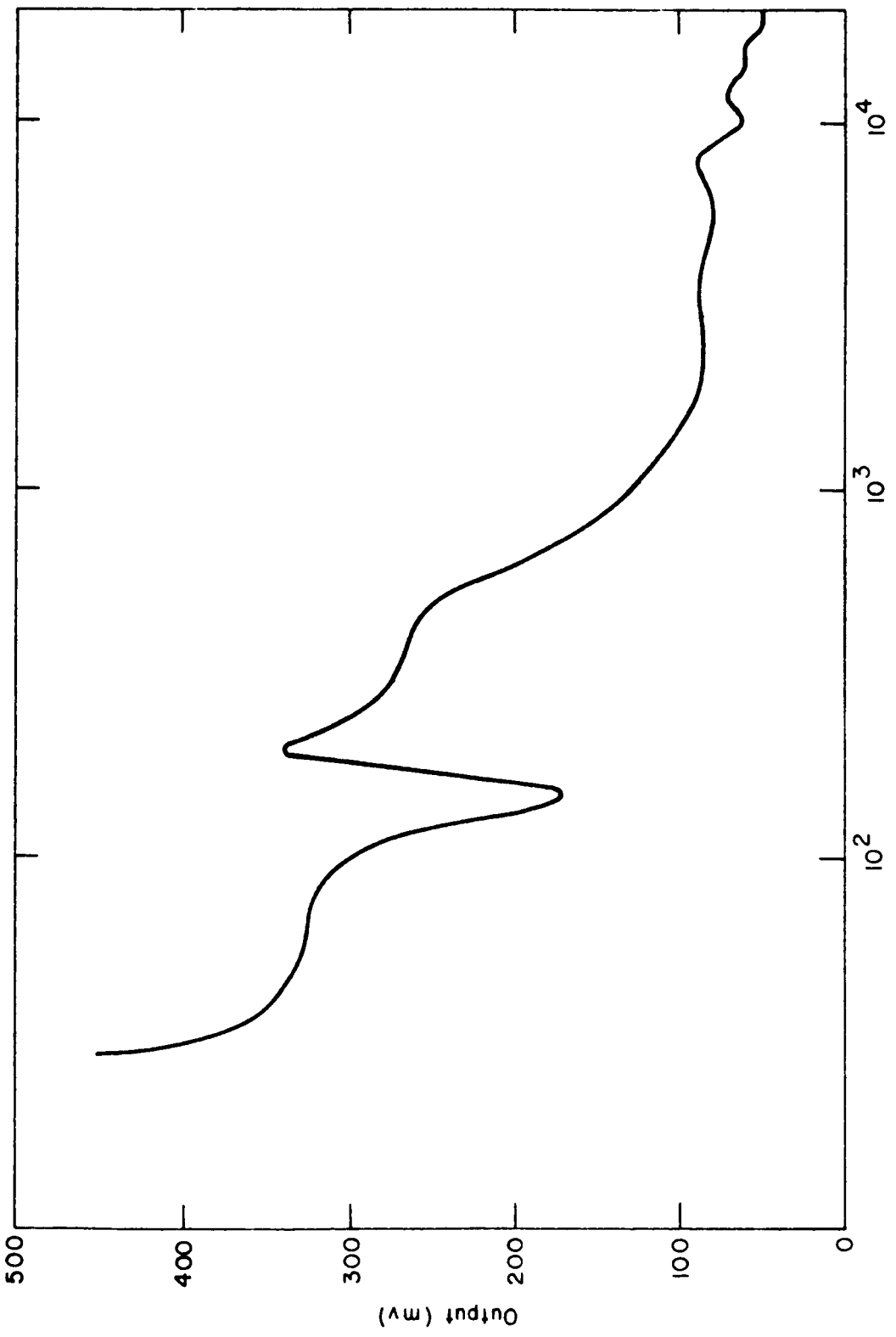


Figure 10 Frequency Response of a Piezo-Transistor Pickup

As a first approach, employing a separate transistor operating in the free-running avalanche mode, we applied stress directly to the shallow emitter-base junction of the avalanche transistor. The oscillator circuit is shown in Fig. 11. As the B^+ voltage is increased, the collector current increases; the voltage buildup across the extrinsic base resistance and the capacitor causes the emitter junction to become forward-biased. The transistor then avalanches, the condensor is discharged, and the process is repeated in an oscillatory manner. Stress on the emitter-base junction changes the time constant of the RC network and thus varies the output frequency of the avalanche transistor. The sensitivities we achieved with this circuit were in the order of 1 cycle/dyn at about 100 kc.

Our next step was an attempt to reproduce these results with an integrated circuit. We chose an integrated circuit which employs a direct coupled logic, and so a scheme had to be worked out to do away with the need for a capacitor. We know that the output capacity of a grounded emitter transistor is a function of beta. This suggests that not only could we do without the capacitor, but that we could make use of the capacity variations which accompany the change in beta under stress. We were able to make capacity measurements, which substantiated these expectations, as shown in Fig. 12. The left-hand part of the figure shows the variation in capacity versus applied stress in grams. The graph on the right side shows the piezo-transistor connected directly to the base circuit of the avalanche transistor. In this case the stress-sensitive transistor replaces the diode and the capacitor of the previous circuit. The relationship between frequency variation with applied stress is seen to depend on the stress level. In the most sensitive region we find a response of about 5 cycles/dyn, which we found to be stable and reproducible within about one percent.

1.4 Physical Aspects

The elucidation of the physical origins of the ASE presents considerable difficulties, mainly because it involves the interaction of several

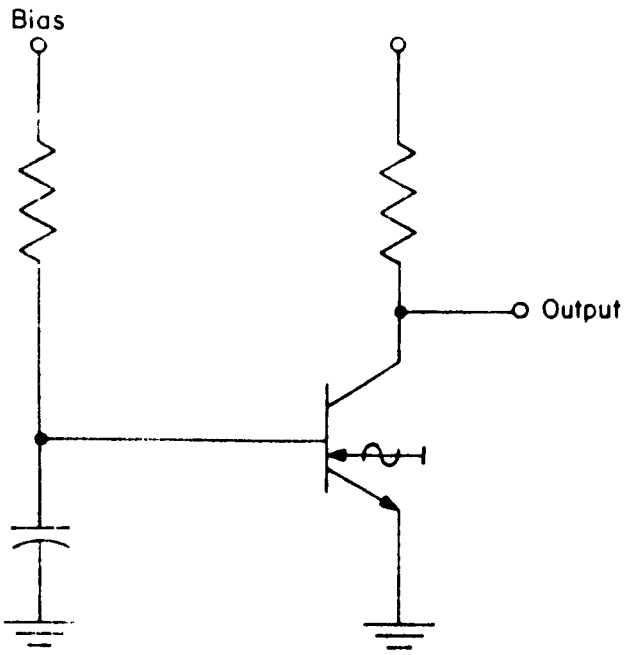
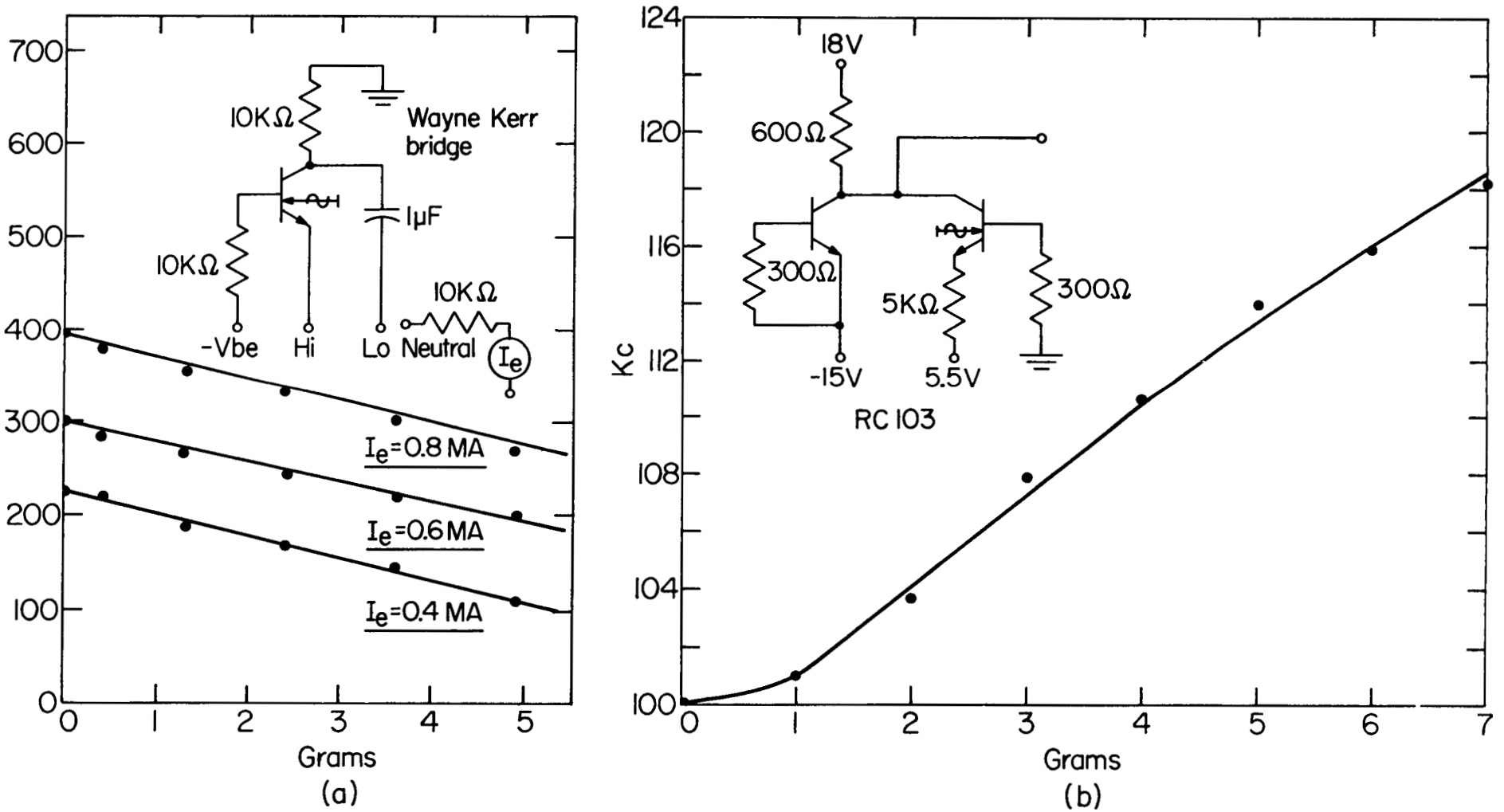


Figure 11 Avalanche Piezo-Transistor Oscillator
(Indicates the Presence and Direction of a Stress Input.)



a. C_{oe}-Stress Relationship of a Piezo-Transistor

b. Frequency-Stress Relationship of an Integrated Avalanche Piezo-Transistor Oscillator

Figure 12 Capacity Measurements

physical mechanisms, each of which individually contributes significantly to the resultant effect. Another difficulty stems from the anisotropy as well as from the large magnitude of the strains involved, which exceed those for which many semiconductor properties are known with certainty.

Of a variety of physical models initially considered in the attempt to explain the ASE, the choice had been narrowed down to two. One model, compatible with the main manifestations of the effect in conventional junctions, was based on a bandgap narrowing under stress.[4,5] Another model, envisioning the creation of generation-recombination levels as a consequence of stress, was also compatible with the manifestations of the ASE in conventional junctions but, in addition, also explained the effect in tunnel diodes in which tunneling through stress-induced states is assumed to take place. In this model the generation-recombination levels were considered to be associated with stress-induced crystal defects. The question, which physical mechanism dominates, was the subject of considerable attention at the time the contract began. Recent work under USAF support has shown that both mechanisms are involved, their relative contributions depending upon the characteristics of the junction and the applied stress field.

1.5 State-of-the Art at Program's Beginning

The semiconductor field over the last decade or so had abounded with effects which, after great initial promise, never reached practicality. If we may anticipate our conclusions, the ASE appeared less and less to fall into this category.

The scientific significance of the ASE was never in doubt once the effect was firmly established; however, the device potential was the subject of considerable controversy. The reservations expressed were partly realistic but partly also strongly tinted by an intuitive uneasiness over the feasibility of ever achieving mechanical control over such a minute and sensitive structure as a piezo-junction. We have already shown that the intuitive

reservations are groundless - the introduction of a stressing stylus on essentially conventional devices had already gone beyond the initial experimental stage, and its feasibility was well established by our device work.

Reservations with respect to more fundamental aspects, however, had to be taken seriously, because they involved incompletely answered questions. In the first place, the semiconductor is subjected to very high stresses and might be expected to yield mechanically and thus alter its characteristics instantaneously or with the passage of time. We had studied this question in some detail and had found that there was a minute permanent deformation of the semiconductor on first contact with the stylus but no evidence of a long-term degradation of the surface when continuously stressed. On the other hand, we did observe fluctuations, the origins of which had yet to be determined. A related question was the problem of noise. The highest sensitivity is generally of little (but not completely without) use if accompanied by substantial noise. The experimental evaluation of the noise level presented a considerable problem, because meaningful noise measurements had to await a sufficient mastery of the new technology to eliminate contact noise due to microscopic stylus displacement. We had reached the point where these measurements could be conducted, and a systematic effort in this direction was under way. A first evaluation of noise limitations could be made from the data that we presented on the piezo-transistor accelerometer.

Temperature dependence of P-J devices had been found to originate mainly from two sources. As determined previously,[2] the ASE as such decreases with decreasing temperature, i.e., under constant stress the stress-induced current drops with temperature. In practice, however, the temperature dependence of the stress bias built into a P-J device depends very much on thermal matching determined by the mechanical configuration and the specific materials used. Thus, a device's over-all temperature dependence was found to be quite complex, and except for the fact that drifts caused by the two effects tend to be additive in the simpler geometries, little was known about this important parameter.

So far, we have discussed P-J devices with reference to only one basic structure - that of a sharp diamond stylus stressing a rigidly supported plane semiconductor surface over a shallow junction. Obviously, many other possibilities exist for converting small forces into high-level anisotropic stresses, since any abrupt change in structural geometry, such as a hole or notch, raises local stresses. For example, a structure consisting of a thin, narrow bar of silicon with a planar junction near one surface and a deep transverse notch on the opposite surface was evaluated by the Raytheon Semiconductor Division. The bar was supported in cantilever fashion, with the junction and its associated stress-concentrating notch close to the clamped end. Forces applied to the free end produced bending, and the resulting stress field produced electrical effects qualitatively similar to those observed in the case of the pointed stylus. Some advantages inherent in this cantilever diode approach are the elimination of the diamond stylus, and a higher compliance, which minimizes alignment and assembly problems in end products. The stylus structure, on the other hand, had been found much more efficient on an energy conversion basis, since equal input forces produced greater electrical outputs; moreover, the displacement of the stylus was a few microinches compared to a few mils for the bar. The high mechanical impedance of the stylus configuration also resulted in devices with higher resonant frequencies, and the circular symmetry was ideal for most transducer applications. Finally, the ease with which stylus-transmitted stresses may be applied to transistors or to single junctions in tiny, high-density integrated circuits had led us to concentrate our initial efforts on the development of that configuration.

We started out with an effect of enormous magnitude, but stable display of it demanded micromanipulators, concrete blocks for stability and insulation against vibrations, and very steady hands. At the start of the subject contract we had packaged units no larger than transistors, which could withstand normal handling and which, in some respects, far surpassed commercial transducers. At the same time, we had become more critical

and needed to know more about noise, about long-term stability, etc. - the investigation of which demanded time and experience. There was no precedent of semiconductors operating at such high stress levels, and this was one reason why predictions were difficult. Looking back, however, and examining what information we have collected so far, there is reason to feel optimistic about the future of piezo-junction devices.

2. BASIC PIEZOTRANSISTOR ELEMENT

2.1 Fabrication Procedures and Yields

The starting point is an uncapped standard silicon planar transistor. For this program the Raytheon 2N2315 was used, which is normally characterized as a fast, high-current switch and is readily available on the TO-46 Microbloc header. The surface over the emitter-base junction is etched in a modified CP-4 etchant to within 1 micron of the junction, and the header is drilled in 2 places to allow subsequent access to the device interior. A modified phonograph stylus 0.030 in. long × 0.015 in. diam. × 0.0005 diamond tip radius is then bonded to the emitter with a crystalline wax, in an area determined to be stress sensitive by micromanipulator probing. This subassembly is then set aside until needed.

A standard TO-18 transistor cap is machined to an over-all height of 0.074 in., and is soldered to a 0.001 in. BeCu sheet. Trimming and plating complete the cap subassembly.

Final assembly is performed by placing a small drop of heavily filled epoxy on the exposed flat upper stylus surface of a previously prepared transistor-stylus subassembly. A cap subassembly is then resistance welded to the header rim by the technique used in conventional transistor production, resulting in a 2-6 mil gap between stylus and diaphragm filled with the uncured epoxy resin. A negative pressure of approximately 6 in. Hg is applied to the diaphragm to pull it away from the stylus, and the epoxy is allowed to cure. When cured, the pressure is released, causing the diaphragm to exert a compressive force on the stylus and stress on the junction. The stylus-jigging wax is then flushed from the can with solvents injected through the previously drilled holes in the header, finishing the basic element.

At the start of the program, approximately 75 percent of the basic elements being produced exhibited useful sensitivity (>1/2 V per gram)

and preload (>1 gram), and showed reasonable gains and leakages. The yield dropped to less than 10 percent shortly after the program began, and a major effort was directed to solution of this problem, since it affected our ability to perform all other required tasks. Most failures were manifested as lack of preload and little or no sensitivity, accompanied by such degraded transistor characteristics as high leakage currents and very low beta. Step-by-step study of all processes did not reveal any single major cause, but tightened control in all areas gradually raised the yield to 80 percent at the time of contract termination. Among the factors found to have caused deterioration were creep in the cap–diaphragm solder joint and shrinkage of the epoxy link to the stylus. One of the major improvements in the process was an operation for correction of insufficient preload, in which the previously welded rim was again passed through the resistance welding cycle several days after fabrication. The very slight displacement thus produced was sufficient to cause preload, the degree of which could be controlled by selection of welding heat and pressure.

2.2 Evaluation

2.2.1 Effect of Bias

The 2N2315 transistors used in the subject contract have the following minimum characteristics:

BVCBO = 60 V (min)
BVEBO = 5 V (min)
ICBO = 1μA (max)
hFE = 40 to 120 at I_c = 150 mA
f αc b = 150 MC (avg)

They are, therefore, capable of operation in a wide variety of circuits. For purposes of standardization we have adopted the circuit of Fig. 13 for all testing purposes, and all measurements reported herein have been made

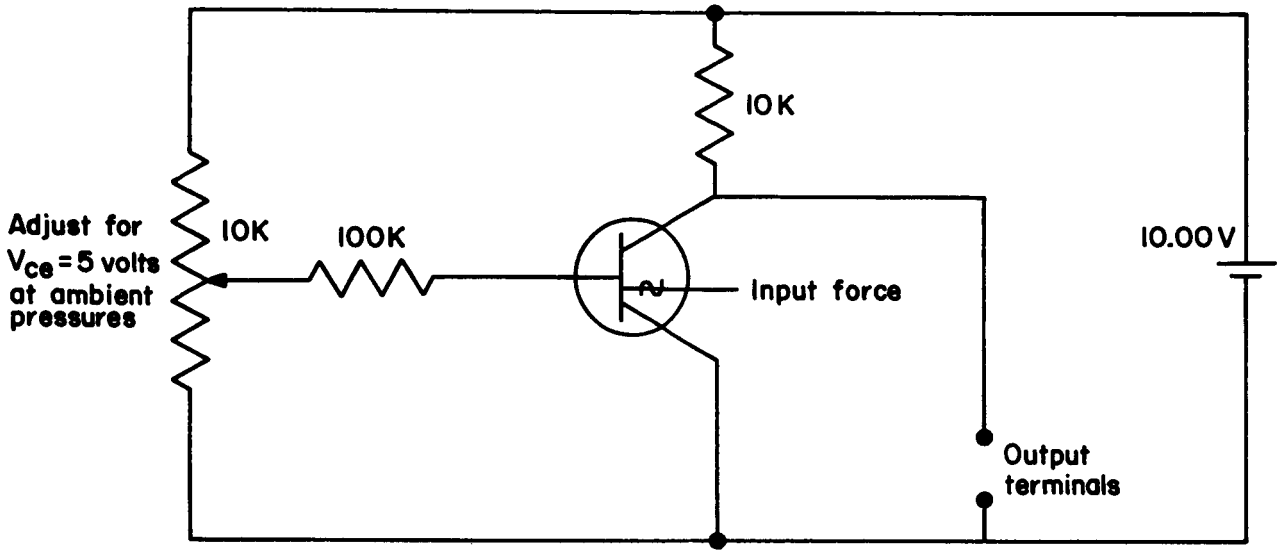


Figure 13 Standard Piezotransistor Test Circuit

with that configuration. It must be emphasized that this was an arbitrary choice, and represented an attempt to gather data that would be useful for practical application and easily repeatible in a circuit of minimum complexity. It does not result in the greatest sensitivity, best frequency response, or lowest thermal shifts. For instance, in an otherwise similar circuit, with VCC = 60V, R_c = 100K Ω, sensitivity is increased by about 5 times. On the other hand, operation with a single 1.3V cell at 100μA current drain is perfectly acceptable for micropower applications, although the sensitivity is an order of magnitude less than that in the standard circuit. Furthermore, the transistor is usable in many digital and linear circuit applications, in which the applied force or pressure can be made to directly change gains, frequencies, voltages, and other parameters which are or can be made dependent on the transistor characteristics modulated by stress. The circuit designer can, therefore, be seen to have a very wide choice of operating modes for injection of the transduced mechanical signal.

2.2.2 Sensitivity, Linearity, Hysteresis

Evaluation of all piezotransistors was performed by application of positive and negative pressures in the apparatus schematically depicted in Fig. 14. The standard is a metal strain gage pressure transducer which is periodically calibrated against a water manometer and resistance calibrated prior to each run. The piezotransistor is in parallel pneumatically with the standard, and the outputs are run to the Y and X axes respectively of a plotter. The conversion factor from pressure to stylus force is 14 in. H_2O = 1 gram.

Reference to a typical piezotransistor characteristic curve, Fig. 15, reveals that the best linearity and sensitivity occur at collector voltages between 1 and 5 V. Sensitivity, defined as the slope of the curve in the center of the linear region, averages approximately 2 V/g and ranges upward to 15 V/g. In general, the more sensitive units tend to have the best linearity and lowest hysteresis. Linearity of most units is within 1 percent over a span of 2 to 4 V, centered between VCE = 2 and 3 V, and hysteresis in this region averages 2 percent of full span. It must be realized that the curves represent

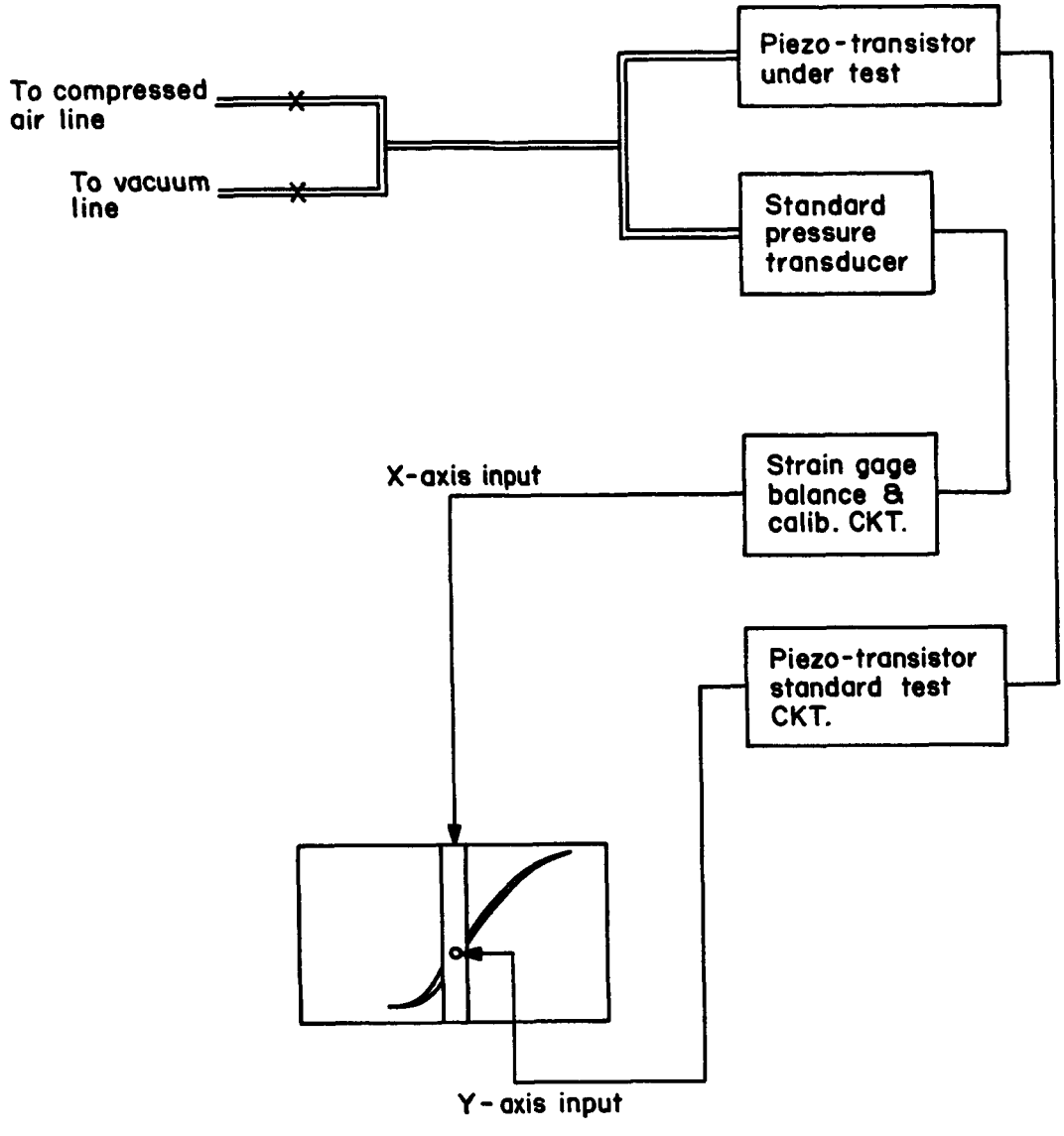


Figure 14 Schematic Representation of Piezotransistor Curve Plotter

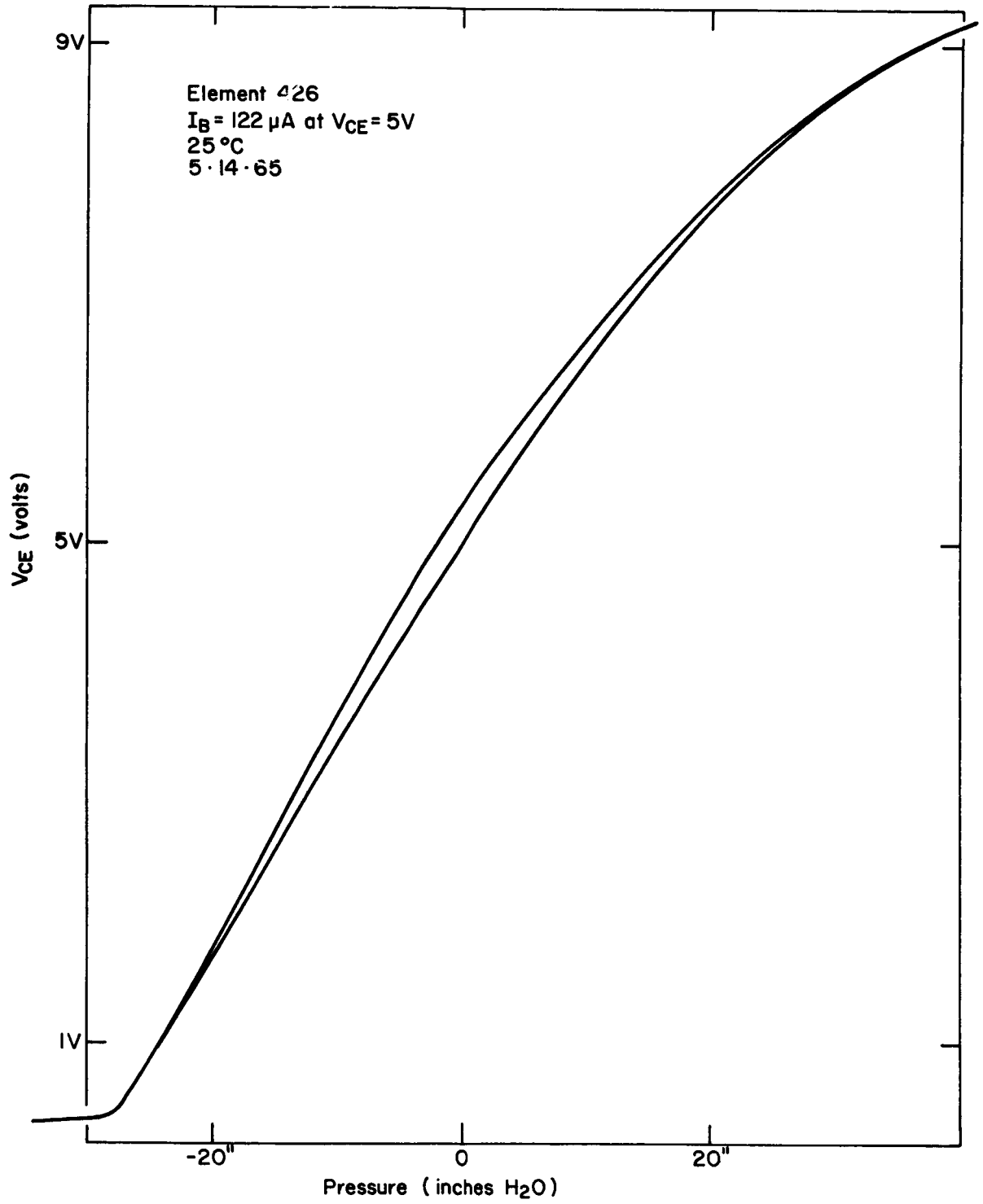


Figure 15 A Typical Piezotransistor Characteristic Curve

very large signal operation, and that hysteresis is considerably reduced when operation is restricted to the linear span. Because the most sensitive piezo-transistors tend also to be superior in most other characteristics it is probable that this behavior represents the norm for an undegraded device, and it is reasonable to expect that further work will result in the ability to achieve this over-all superior performance on a regular basis.

2.2.3 Preload

Because the characteristic curve describing the ASE is S-shaped, as can be seen in Figs. 3 and 12b, stress bias, or preload, is necessary to place the "dc mechanical operating point" in the region where sensitivity and linearity are optimum. The preload magnitude is not particularly critical, since levels from 1 to 5g have been measured in excellent devices; however, it has proven difficult to sufficiently control preload to even this wide tolerance. The minute (a few microinches) displacement of the stylus into the semiconductor and the small size of the entire structure compound the problem, for it is not practical to use such conventional approaches as screw-adjusted springs, etc. Furthermore, even momentary application of high stylus forces (5 to 15g depending on the configuration) causes permanent damage and results in little or no sensitivity and very degraded transistor characteristics.

The displacement of the diaphragm center from a flat condition is less than 0.0005 in., with a probable allowance of ± 0.0002 between insufficient and excessive preload, and is reduced if the diaphragm is not perfectly flat initially. The inexactness of the foregoing statement arises from the fact that small and unpredictible differences in solder fillet size, diaphragm thickness, and diaphragm tension strongly affect the already inexact expressions relating forces and displacements of such structures. Fortunately, the rewelding procedure developed during the latter part of the contract has enabled us to control preload to an acceptable degree in the basic element, but incorporation into accelerometers and other practical transducers requires due consideration of the change in preload caused by connection of additional structure to the element's diaphragm.

2.2.4 Behavior with Temperature

Several piezotransistors have been repeatedly exposed to 90°C temperature with little evidence of damage, although 2 of 4 units failed at 105°C. We feel, therefore, that the present design is limited to temperatures below 100°C. It should be possible to attain 150°C operation with the present silicon transistors in an improved structure, but drift will undoubtedly be a major problem. Figure 16 depicts a typical temperature run on element 307, which has been so exercised 11 times with little change in characteristics.

In the present piezotransistor, an increasing temperature causes reduced stylus pressure, primarily due to expansion of the diaphragm, which is initially dished outward because of the stylus pressing against its center. Unfortunately, the resulting increased collector current reinforces the inherent collector current change which every transistor exhibits under increased temperature. While we recognized very early the desirability of providing a package which caused increased stylus force with rising temperature, the other constraints on package design eliminate many approaches. Two which seem compatible are a bimetal diaphragm and a diaphragm with a formed concave upper surface. The bimetal diaphragm, while not yet investigated, may well prove satisfactory. Preliminary tests with concave diaphragms resulted in inoperative elements, due no doubt to the reduced compliance of such a geometry. Very recent work, however, has shown the feasibility of assembling the element without any attempt at preloading by reduced pressure, rather preloading by rewelding after completion of fabrication. Several elements so produced have shown negative temperature coefficients, illustrating that some lesser concavity could indeed eliminate temperature drift, at least over a limited range. This promising avenue should be further investigated in the future, for small residual drifts could be electrically compensated by techniques analogous to those used with metal or semiconductor resistive strain gage transducers.

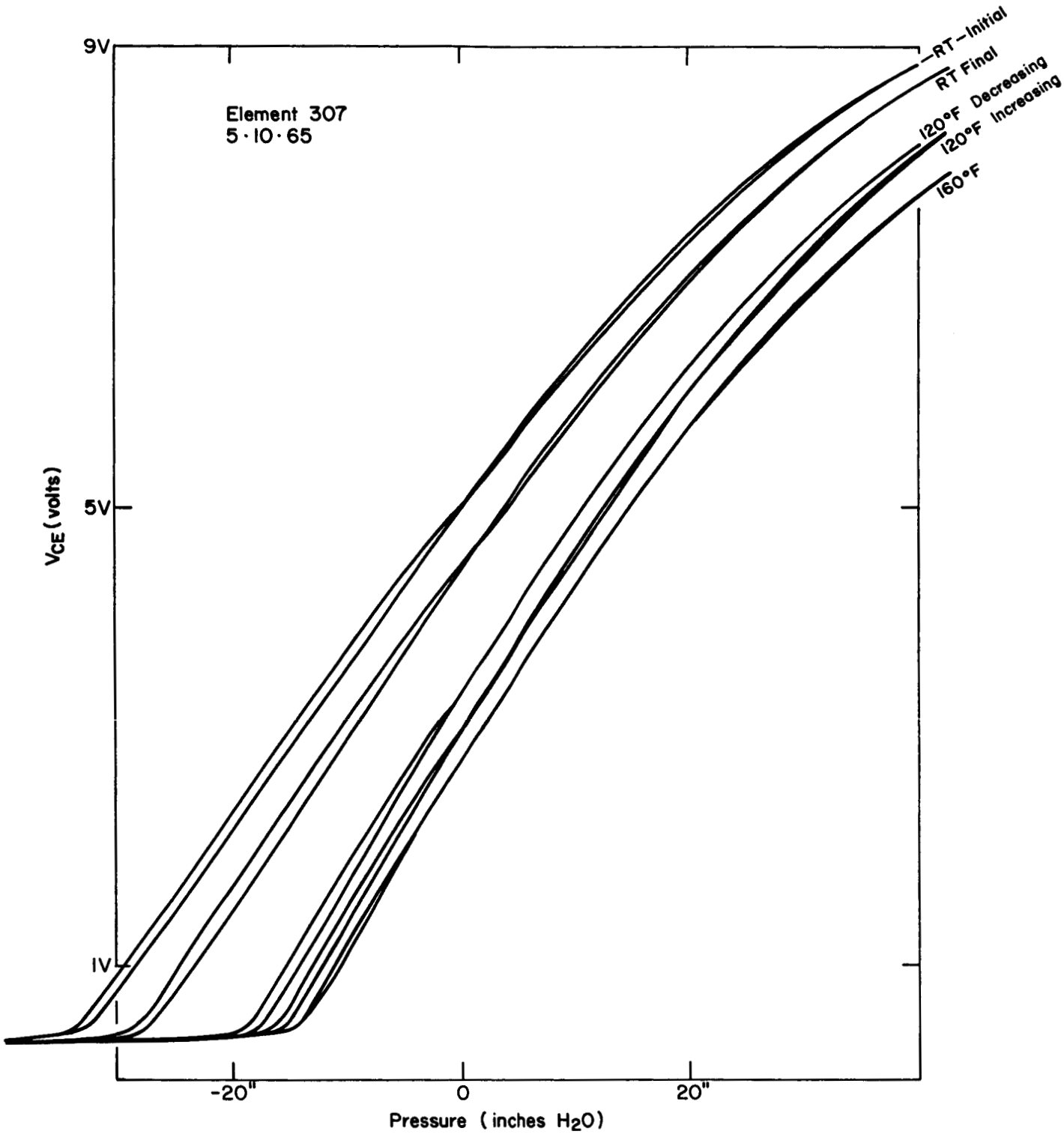


Figure 16 High Temperature Characteristic Curves of Element 307

2.2.5 Life

Extreme variations have been encountered in the life of piezotransistors. Some individuals have now remained essentially unchanged over periods of up to a year, despite frequent handling and exposure to various test conditions, while others fail catastrophically or deteriorate gradually over intervals of a few days to a few weeks. Certainly the continuous exposure of the transistor to external environments results in degraded junctions, for the passivated layer is removed during the initial etching procedure, and the exposure to solvents and other contaminants during processing violates fundamental requirements for semiconductor reliability. While we recognize these as problems with obvious solutions, we have chosen to defer these to future programs, inasmuch as the more crucial problem of fabricating devices with acceptable yield is just now nearing solution. Use of passivated transistors with junctions sufficiently shallow to eliminate the need for etching would avoid most contamination problems during processing, and hermetic sealing of the finished piezotransistor would avoid subsequent entry of foreign substance. Unfortunately we have been unable to locate standard passivated transistors with suitable shallow emitter-base junctions, although such are within the present state of semiconductor device art. Furthermore, hermetic sealing of the finished piezotransistor, while eminently possible in theory, will require a considerable amount of work for reduction to practice. Our earliest elements were hermetically sealed at atmospheric pressure, but we found such extremely high thermal drifts (of the order of 1 V/F°) due to expansion of the trapped air that they were completely useless as anything except thermometers. A straightforward evacuation of such elements to eliminate thermal sensitivity would have produced stylus forces of approximately 30 g, resulting in destruction of the stressed junction. Obviously, the requirement is for some construction technique which will result in 1 to 5 g force being produced on the stylus when the interior is evacuated, and several such schemes have been devised. Again the matter of priority has dictated that the necessary development take place in the future.

Because, as initially pointed out, some individual elements have demonstrated long life, it is felt that there is no substantial inherent limitation; however, until further research is performed we must regard the life expectancy of individual piezotransistors to be highly unpredictable.

3. INTEGRATED BRIDGE

3.1 Introduction

As a possible approach to thermal stability, with a simple zero-center analog output, a bridge circuit might be employed. Figure 17 shows the bridge circuit schematic. This circuit was converted from a dual NOR gate, Raytheon type RC 322. Since all the elements of the bridge with the exception of the two base resistors are formed on the same single crystal of Si the thermal tracking should be good, and low drift should result. The selection of the dual NOR gate was an attempt to utilize a configuration which required the least amount of modification to fit the needs of the bridge circuit. Some time was spent on the development of techniques and skills to obtain the desired circuit modification by changing interconnections and suitably decreasing the junction depth in the transducing transistor.

Temperature measurements on the integrated circuit before capping show a good null stability with temperature, but the capped bridge element's characteristic is determined primarily by geometrical factors and is essentially similar to that of a simple piezotransistor.

3.2 Circuit Processing

An integrated circuit type RC322 dual NOR gate was chosen. It contained the required number of circuit elements needed to make a bridge. These two base resistors were made adjustable for bridge balancing with one common 10 V power supply. The chips without leads attached were ordered from Raytheon's Mountain View Semi-Conductor Division. The chips were mounted on TO-47 8-lead headers.. The leads were attached to the chip by thermocompression bonding. A standard thermocompression bonding point may be seen in Fig. 17b. This bonding point performs satisfactorily for conventional bonding to the periphery of the chip.

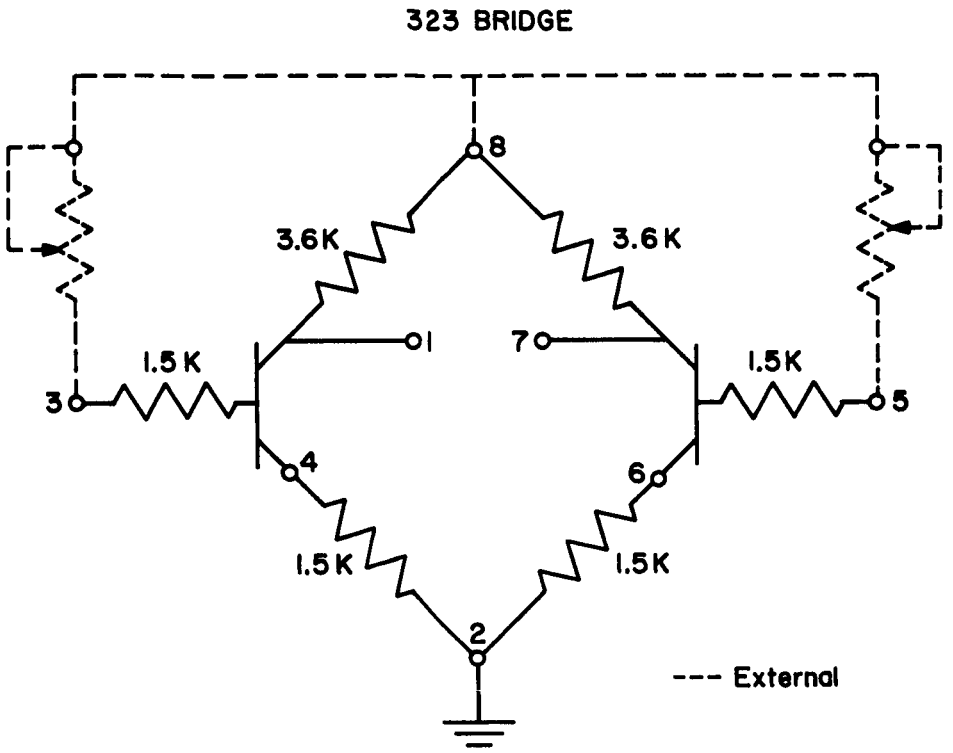
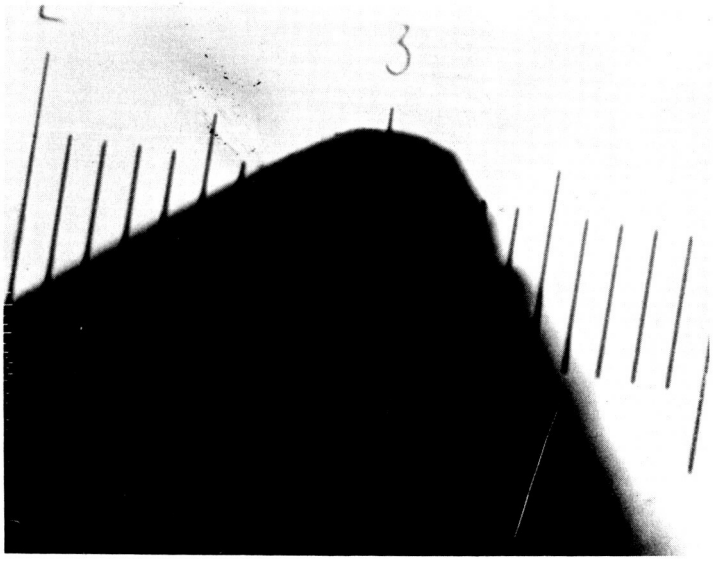
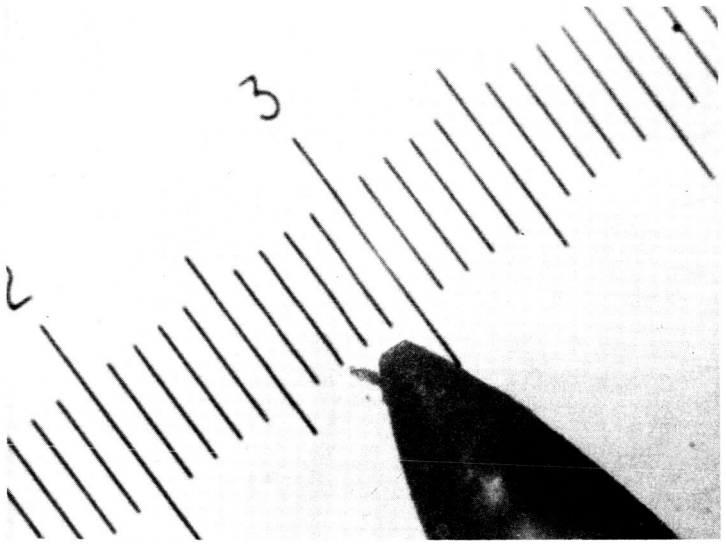


Figure 17a Schematic of Integrated Bridge



b



c

Figure 17b and 17c Photographs of Steel Stylus Used in Bonder

However for the necessary internal connections to the emitter areas ($\sim$ 1/2 $\times$ 1 mil), a small bonding point had to be used. A steel Recoton needle was etched electrolytically in 50 percent HCL and water to obtain the necessary small point radius. Figure 17C shows the resulting needle profile. Also, the small shank of the steel needle allowed for a better view of the emitter during the bonding process. An earlier method involved etching in HCL to remove the Al around the emitter on the integrated chip. This resulted in a poor yield because the HCL had a tendency to creep under the mask and destroy the Al connection to the emitter. By employing the steel needle with its sharp point, the Al could be scraped off in a much more controlled manner. The circled area in the picture of Fig. 18 shows the bared emitter area. Also shown in Fig. 18 is the modified chip.

3.3 Device Fabrication

The next step in the fabrication process is to attach the stylus to the sensitized area. This is done on a micromanipulator locating the stylus in the most sensitive area. The header is then heated and wax is allowed to flow around the stylus. Figure 19A shows the stylus attached to the chip. In order to remove the wax after the unit has been packaged, notches are cut in the header (Fig. 19B). The completed device is shown in Fig. 19C with the diaphragm cap being welded onto the header.

3.4 Temperature Tests on Uncapped Bridge

The first set of measurements on the integrated circuit under elevated temperatures were the measurements of h_{fe} of each of the transistor elements. The tracking of these transistor elements may be seen in Fig. 20 from 25° to 100°C; the match is better than ten percent.

The test was conducted by immersing the integrated circuit and header in Si oil and then heating. The temperature of the oil was allowed to stabilize before each temperature measurement.

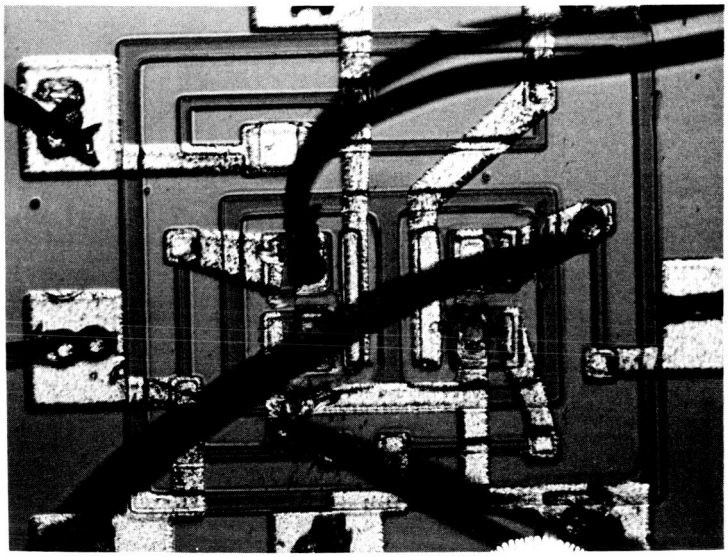
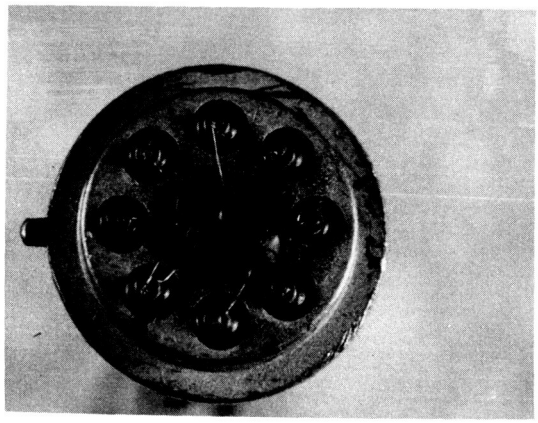
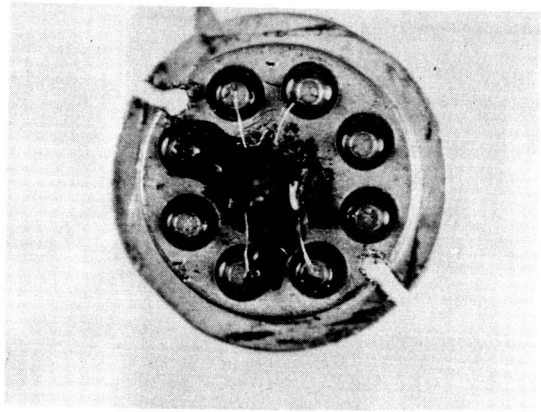


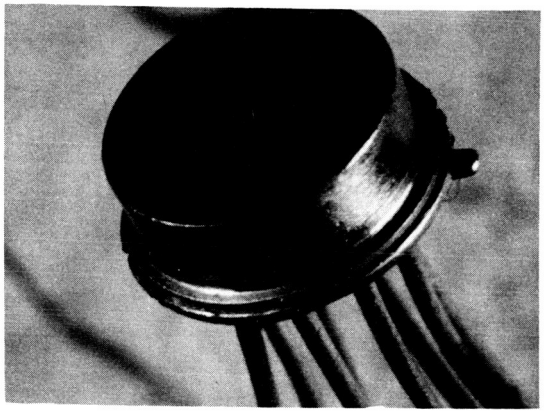
Figure 18 Photograph of Integrated Circuit After Modification



A



B



C

Figure 19a, b, and c Photographs of Successive Stages in Construction

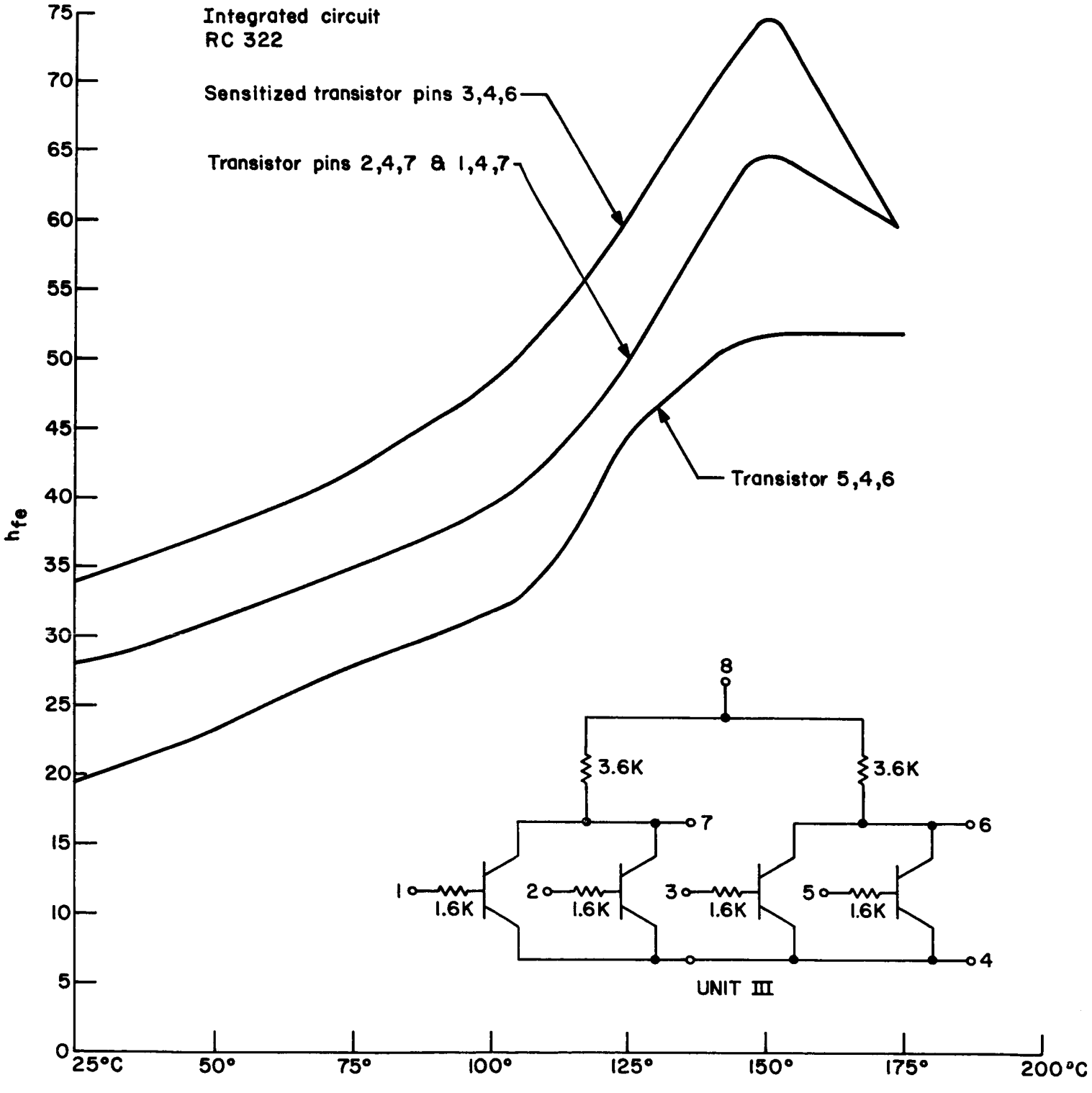


Figure 20 hfe vs Temperature of Three Transistors on the Same Integrated Chip

The configuration shown in Fig 17 was immersed in Si oil and a temperature run made by heating the oil to the desired temperatures. Figure 21 shows the null variation of the integrated bridge circuit. The null drifts to a peak of 7 mV at 65°C, returns to zero at 95°C, and goes in a negative direction very rapidly above this temperature. Beta is increasing very rapidly here, which may account for the rapid change in bridge null.

3.5 External Biasing

Two external base resistors are employed to control the base current in the two transistors which make up the bridge (Fig. 17).

In order to balance the collector currents of the two transistors and thus achieve a null between their collectors, the base currents must be adjusted by varying a power supply or varying the base resistors; the latter was employed thus allowing for one common 10 V power supply.

Figure 22A shows the null vs the variation of R_2 (the base resistor in the base of the nonsensitized transistor). The base current in the sensitized transistor (Ib_1) has been set to 100 μA. (This is an arbitrary setting which has been found to let the sensitized transistors operate in the most linear fashion.) By varying the base resistor R_2 (12 kΩ - 19 kΩ) the base current varies from 400 μA to 280μA. The shift in the null is ± 60 mV.

Figure 22B shows the null shift when R_1 and $\pm b_1$ are varied over a range of 30kΩ to 80 kΩ. The null shifts from +70 mV to -5 mV. The reason of the low minus shift is due to the low beta at 70μA. As stated previously the null has been set close to zero at 100μA. The null is less critical on the sensitized transistor side due to the higher values of base resistance.

3.6 Sensitivity Characteristics

Figure 23 shows the sensitivity of typical integrated transistor, and Fig. 24 shows the sensitivity of a typical integrated transistor with no preload. Figure 25 shows the sensitivity of an integrated transistor after reweld.

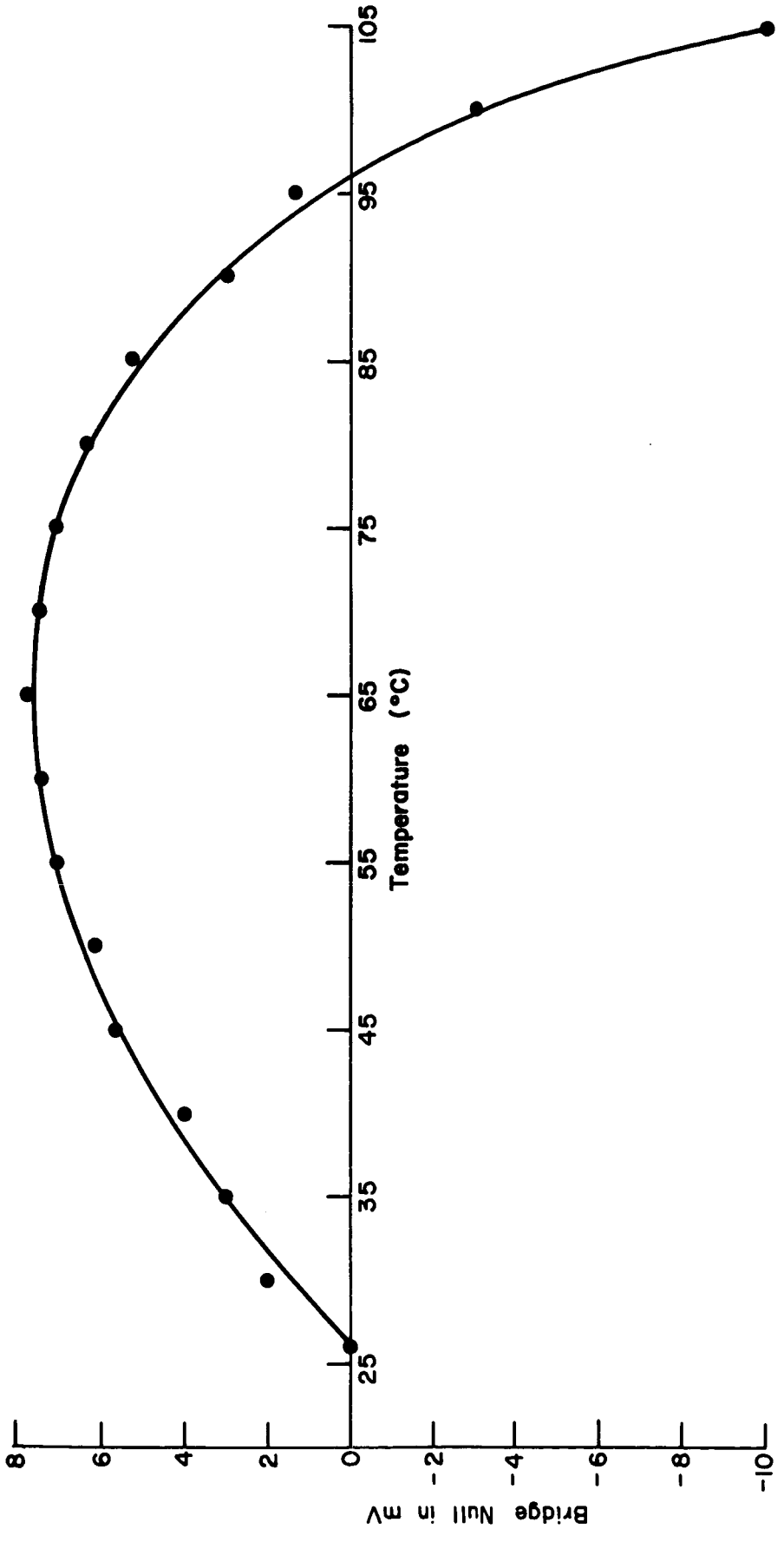


Figure 21 Null Drift vs Temperature

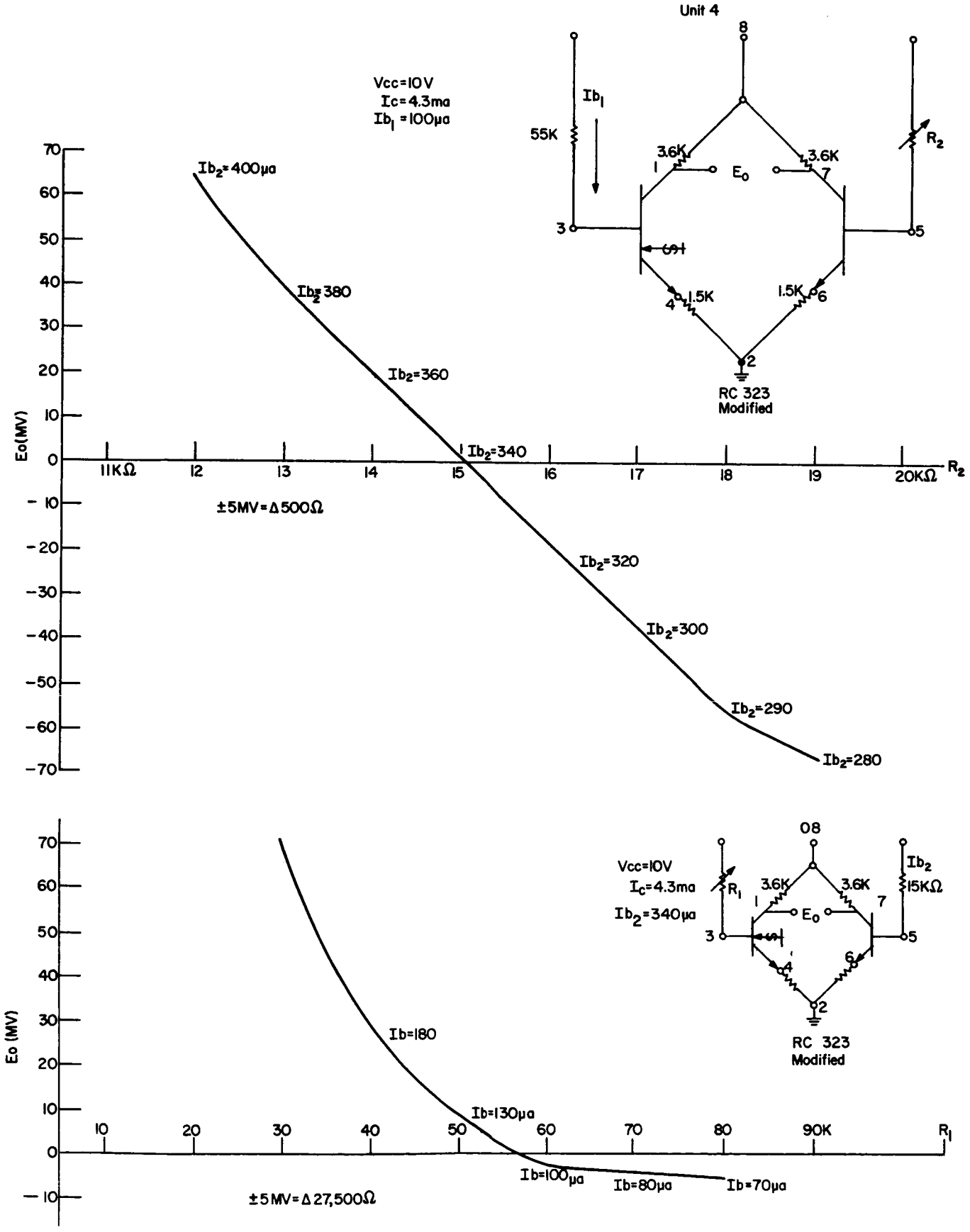


Figure 22a and b Base Bias vs Null Shift

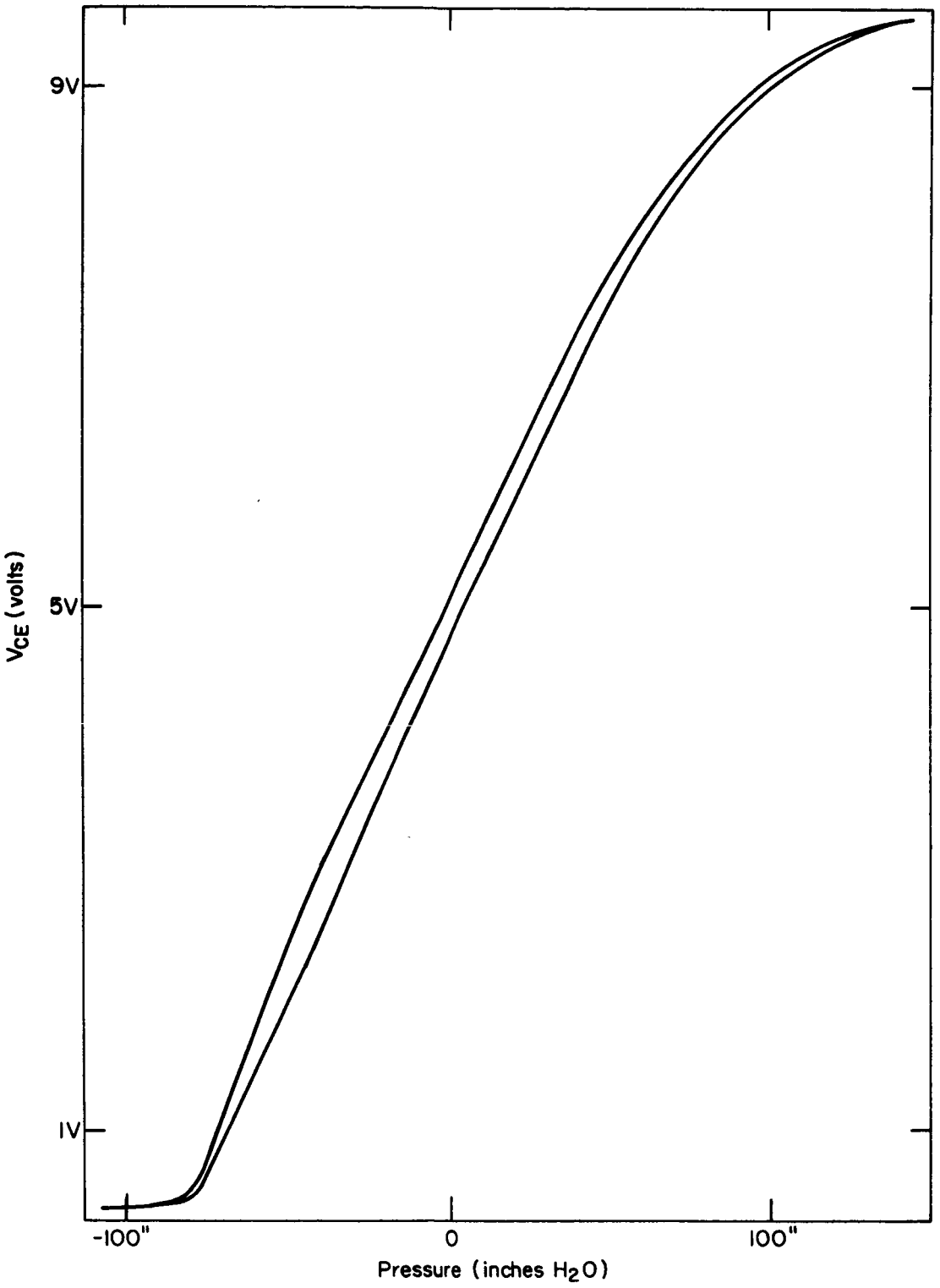


Figure 23 Integrated Transistor Sensitivity Curve of a Packaged Device

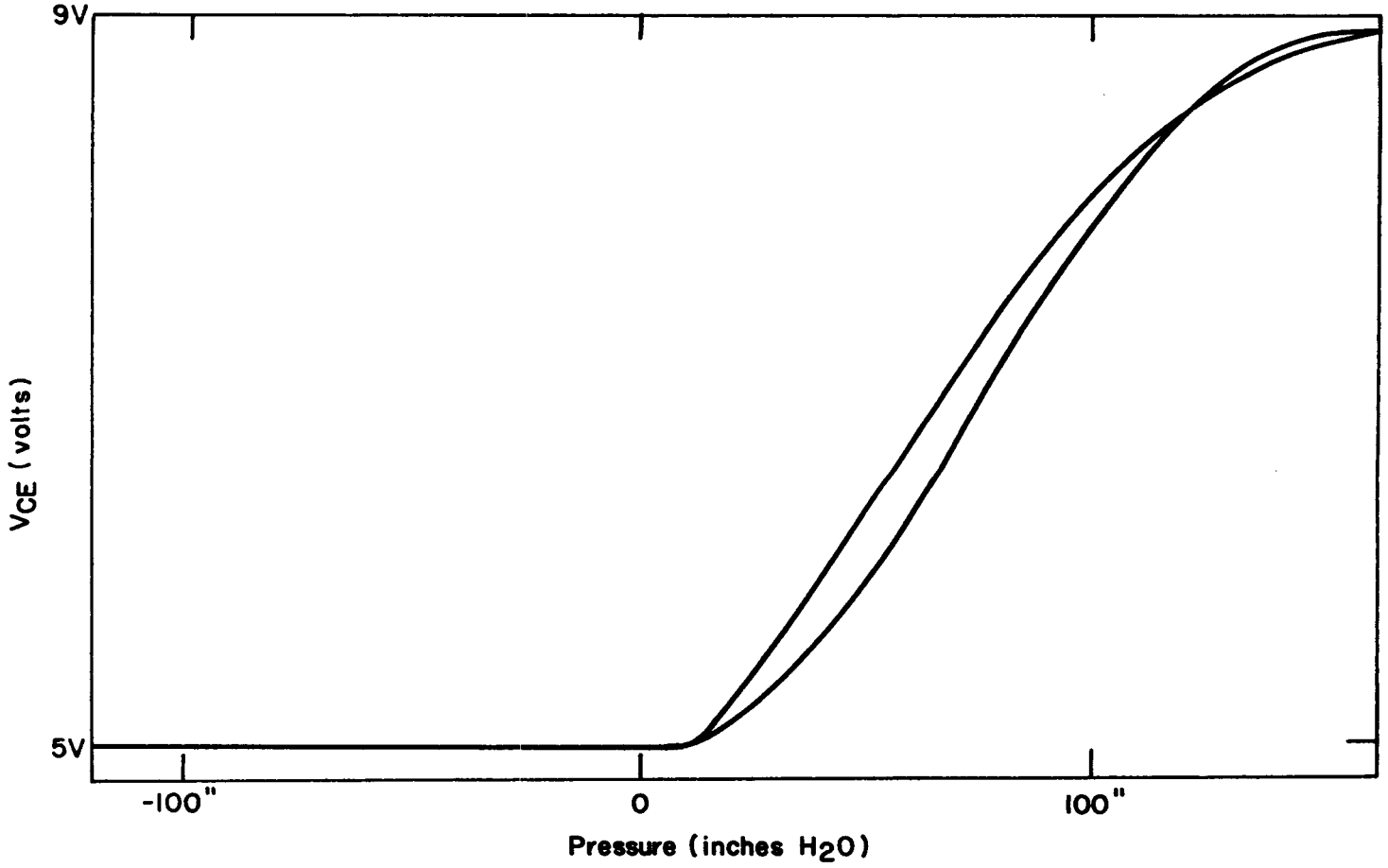


Figure 24 Integrated Transistor Sensitivity Curve with no Preload

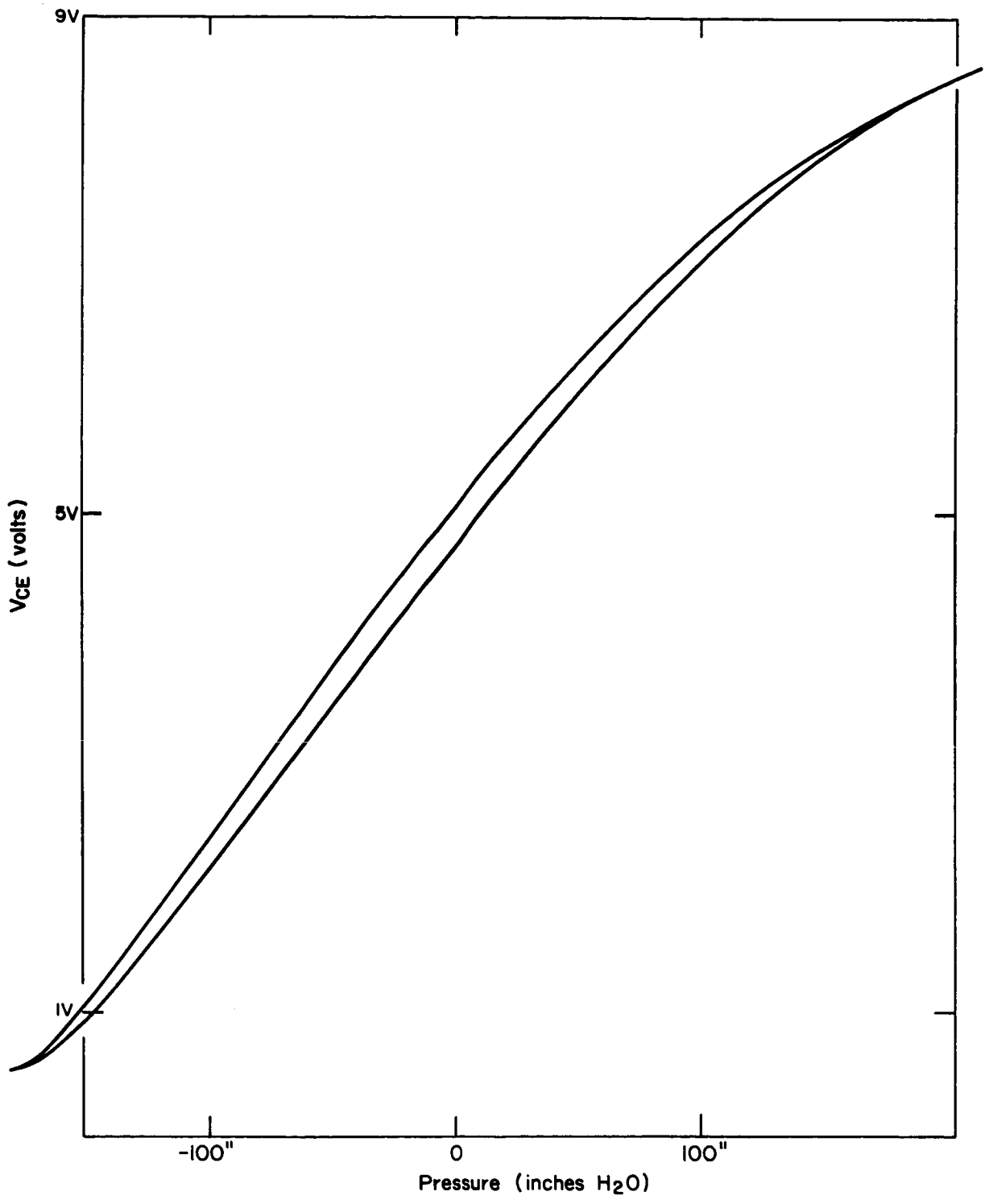


Figure 25 Integrated Transistor Sensitivity Curve After Re-Weld

Figure 26 shows the sensitivity characteristic of a completed bridge. The base current for the sensitized transistor portion was set to 100μA; the other transistor was balanced or nulled against the sensitized transistor. The linearity over a 3 V range is better than ±2 percent with a sensitivity of 0.4 mV/dyn.

3.7 Null Stability of Integrated Bridge

The short-term null stability may be seen in Fig. 27. The null output out of the integrated bridge was monitored for 10 minutes every hour for 5 hours. The bridge was balanced initially. One hour later, the bridge null had drifted to plus 40 mV; the temperature had gone up 1°C. Five hours later, the bridge output was 45 mV; the temperature was up 0.5°C. The temperature stabilized, with the output of the bridge staying at approximately 40 mV. The bridge noise appeared to be within ±5 mV.

The long-term stability (2days) may be seen in Fig. 28. The temperature (1), bridge output (2), and power supply voltage (3) were plotted on a recorder. Positive and negative pressures of 1 in. Hg were applied to the bridge element's diaphragm. Each small division is equal to 10 mV on curve 2. The one inch of Hg causes a change in the output of approximately 0.25 V. The changes in the temperature are shown on Curve 1.

The bridge output changes noticably with temperature, whether under stress or not. Three small divisions indicate 1°F change in temperature. One degree F change in temperature causes about 30 mV, which is in agreement with the change found in the short-term drift experiment.

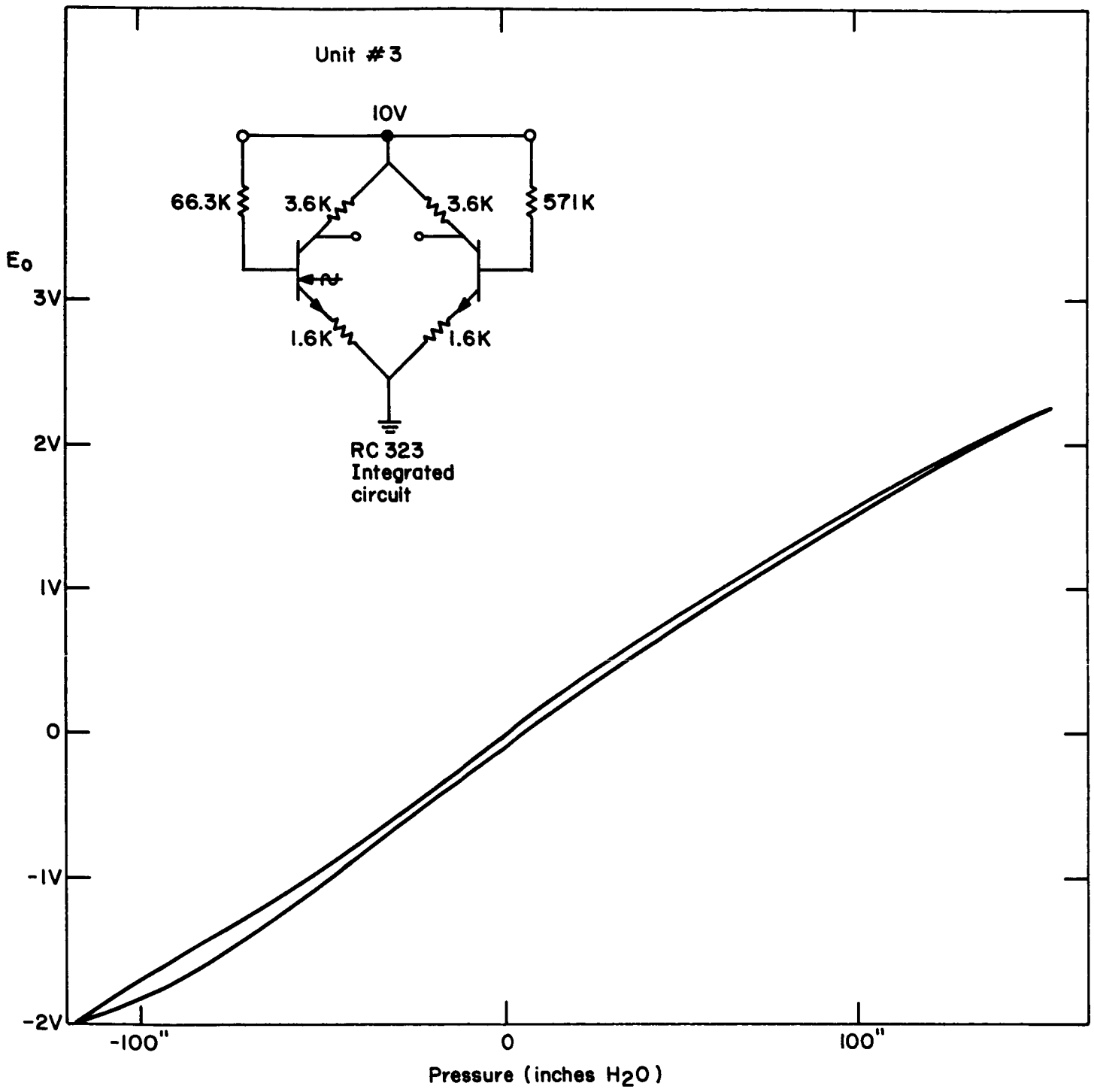


Figure 26 Integrated Bridge Output vs Stress

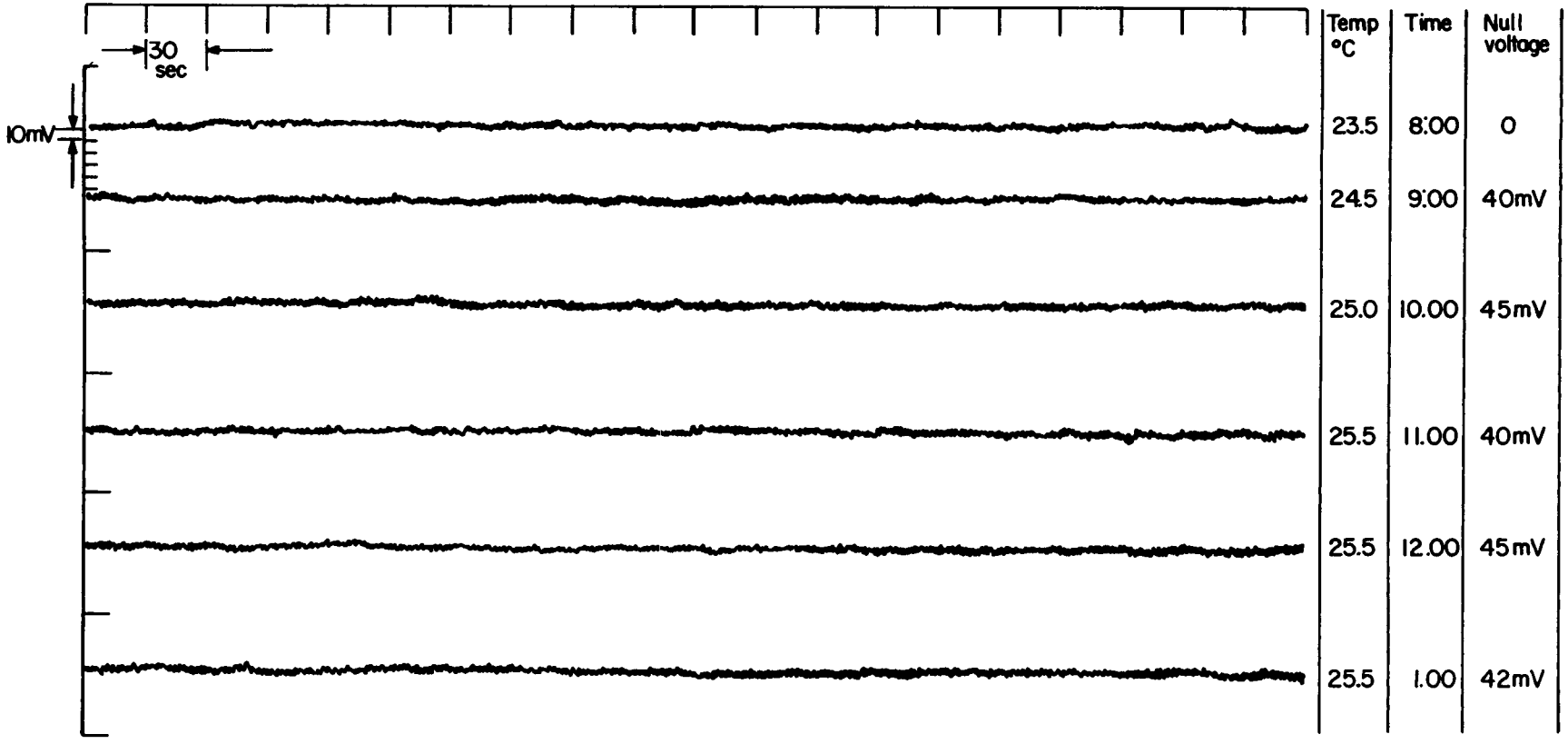


Figure 27 Short Term Stability

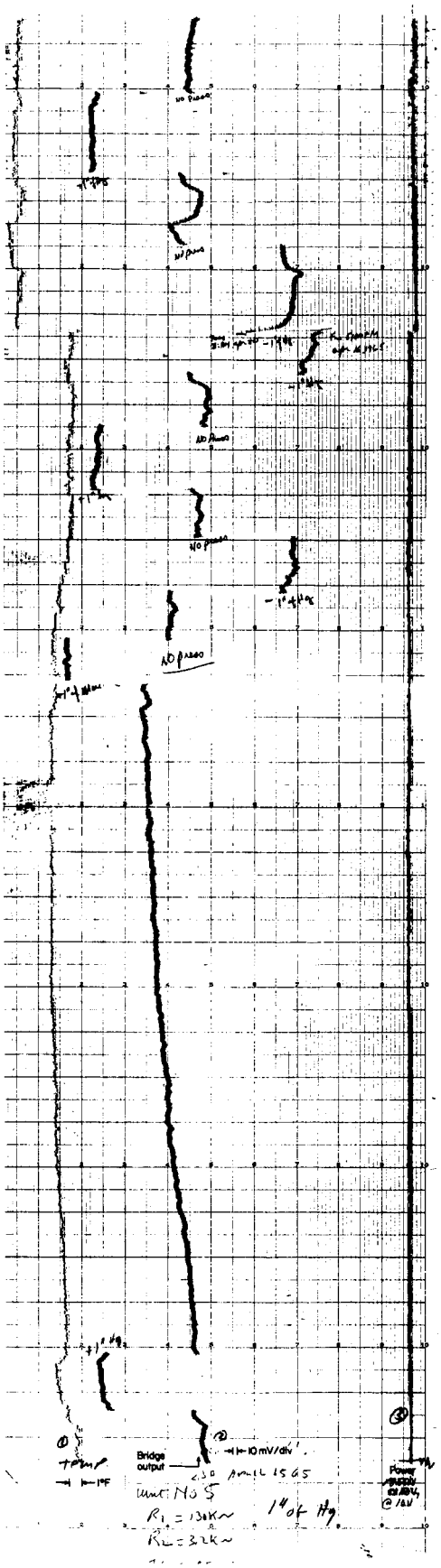


Figure 28 Long Term Stability

4. PIEZOJUNCTION ACCELERATION SENSING ELEMENT

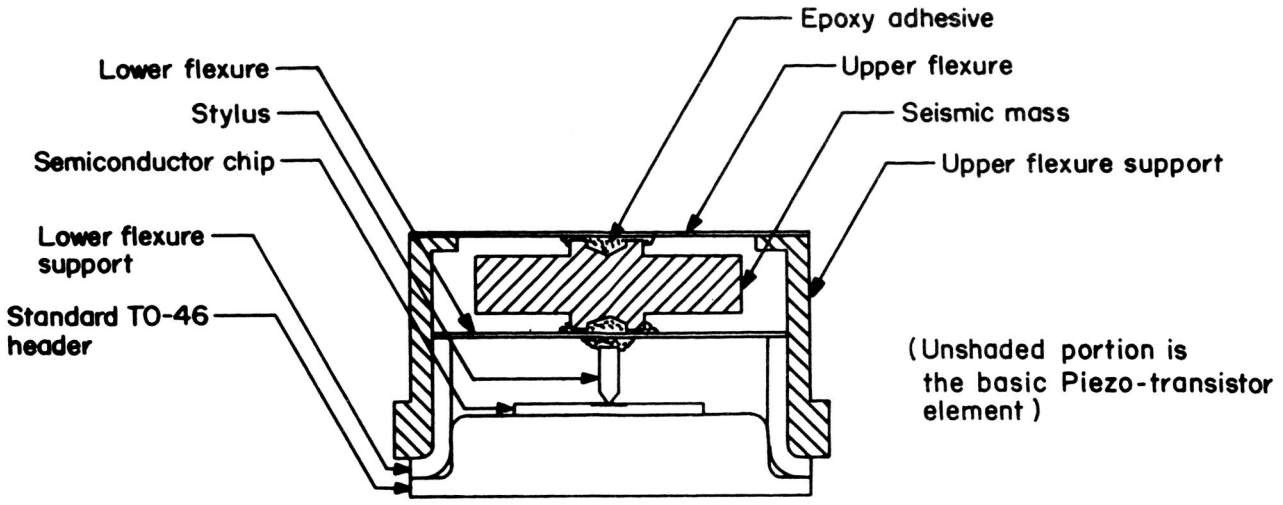
4.1 Design and Fabrication

4.1.1 Design Objectives

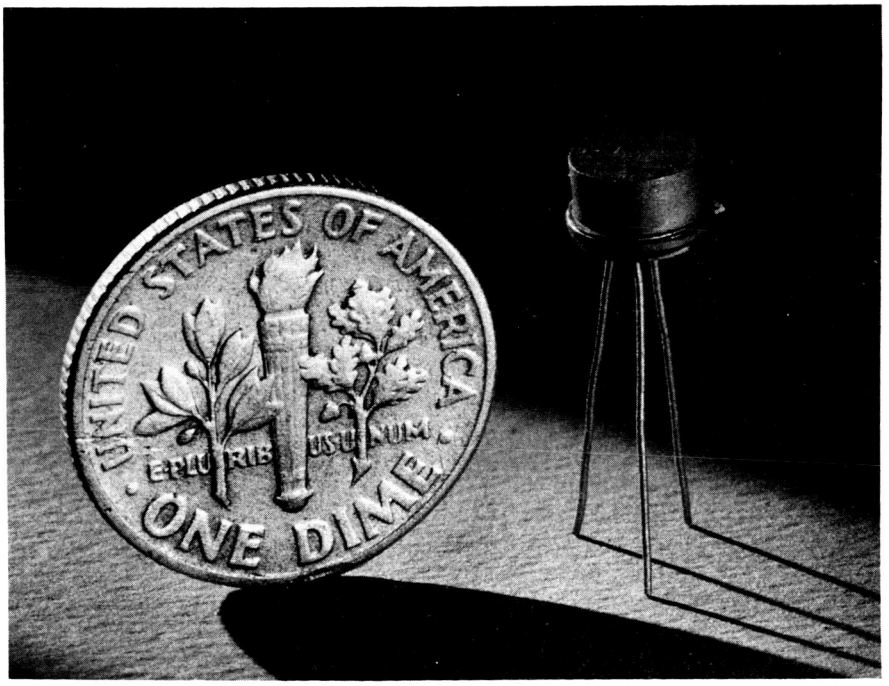
We shall use the terms "acceleration sensing element" or "acceleration sensor" to identify that portion of an accelerometer in which is accomplished the actual transduction of accelerations into electrical form. We shall restrict "accelerometer" to a packaged instrument which incorporates, in addition to the sensor, some means of environmental protection, a means of convenient mounting to a test specimen, and a convenient means of electrical connection.

To convert a basic element, which is a force sensor, into an acceleration sensor, it is merely necessary to apply Newton's second law, $F = MA$, by adding a seismic mass. The mass must be highly constrained laterally but free to move axially. Simplicity is a virtue in all accelerometer structures, since every member adds possibilities for resonances within the operative frequency range; furthermore, the simplest structure usually possesses greatest strength and least weight, both of utmost importance in the application. An additional requirement in our case is that no fabrication step should result in application of stylus forces exceeding 5 grams, even in the form of very short pulses, to avoid junction damage.

The structure of such an acceleration sensor is shown in Fig. 29. The seismic mass (0.05 g in our latest sensors) is suspended between 2 diaphragms of 0.001 BeCu which provide great lateral constraint and by virtue of axial symmetry result in a system free of the modal coupling encountered in cantilever suspensions. Despite the stiff suspension, the governing axial compliance in the mechanical system is that associated with the elastic penetration of the stylus into the semiconductor, which is several orders of magnitude lower than the axial flexure compliance. The sensitivity of the resulting acceleration sensing element, in units of volts per G, can be found by simply multiplying the basic element's force sensitivity by the weight of the seismic



(a)



(b)

Figure 29 Piezotransistor Acceleration Sensor

mass. Although our early acceleration sensors failed by more than an order of magnitude to meet this calculated sensitivity, the most recent attempts have been more successful, and we are now able to achieve 50 percent of the theoretical value. Because the noise level tends to be constant, this also means that the signal-to-noise ratio has improved proportionally.

In applications where minimum size and weight are paramount, and where the environment is benign, the sensor could be adhesive mounted by its flange or outer cylindrical surface, and its 0.5g weight may make it attractive for such purposes under well-controlled conditions.

4.1.2 Fabrication Procedure and Yields

The assembly of an acceleration sensor, using a good basic element as the starting point, is in theory a very simple and straightforward process. One merely solders or welds a thin metal diaphragm to the top of a machined cylinder and bonds thereto a seismic mass, holding the parts in a simple fixture while the adhesive cures. The resulting subassembly is then bonded to a basic element with an epoxy adhesive around the flange, while a small drop of the same adhesive bridges the gap (2 to 6 mils) between the bottom of the mass and the top of the basic element's diaphragm. The structure is self-jigging and requires only a small weight to maintain flange-to-flange contact during the room-temperature curing cycle. After preliminary electrical checks the leads are cut short, fine leadwires are welded or soldered to the stubs, and the header indexing tab is cut off to allow insertion in the holding fixture, as depicted in Fig. 30.

In view of the simplicity of the process, it was difficult to understand the low yields encountered during the major portion of the contract, for the failure rate approached 90 percent. We have now determined that overstressing, caused by extremely short high amplitude mechanical shocks, was the cause of the problem, for the high resonance frequency and low mass of the sensor constitute an ideal system for absorption of such energy. We had early suspected that clipping of the leads and tabs could be causing the observed

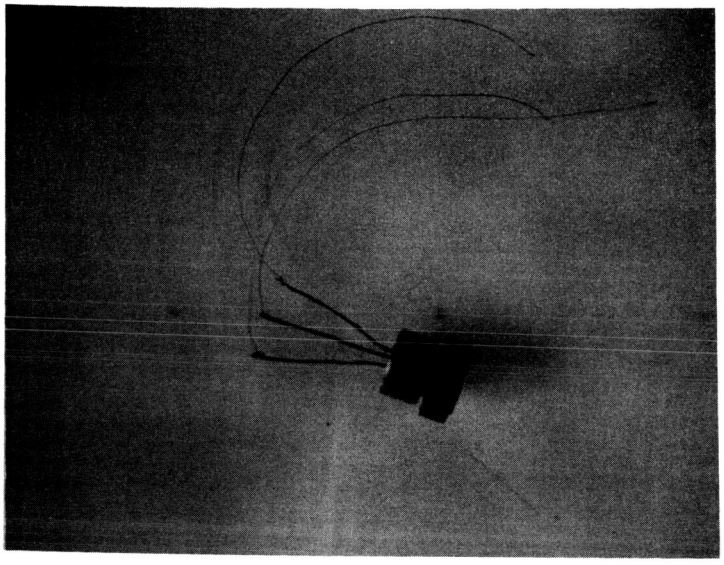


Figure 30 Piezotransistor Acceleration Sensor Mounted for Vibration Calibration

malfunctions, so we switched to a shearing-action cutter and finally to an extremely sharp miniature end cutter for this operation. Using the latter tool, no discernible "snap" is produced and the cutting sensation can be described as "mushy", yet the high failure rate continued. We investigated all other aspects of the process before returning again to the lead and the tab cutting operations. It was only during the final month of work that we pinpointed the cause of difficulty in the trimming of the tab and leads, and this has now been definitely identified as the cause of most malfunctions. By simply performing these operations prior to final assembly, we have had no failures in our last five attempts.

4.2 Evaluation

4.2.1 Standard Test Procedure

The acceleration sensor in its holding fixture is mounted to the table of a high frequency vibration exciter and connected into the standard test circuit of Fig. 13. The base is connected to the bias supply by the center conductor of a coaxial cable, while the emitter is connected to the shield. Up to 1000PF of cable capacitance can be tolerated without affecting high frequency response, and extraneous pickup is reduced to levels below circuit noise. The collector need not be shielded.

The system shown schematically in Fig. 31 maintains a constant ($\pm$2%) acceleration (typically 1G) while the frequency is slowly swept from 20 Hz to 10 kHz. The output (VCE) of the piezotransistor is recorded on the frequency-synchronized recorder chart, and in addition the 100 Hz output is determined by VTVM at 0.1G, 1G, and 10G input levels. The built-in standard accelerometer has a resonance frequency of 140kHz and is periodically calibrated by optical means.

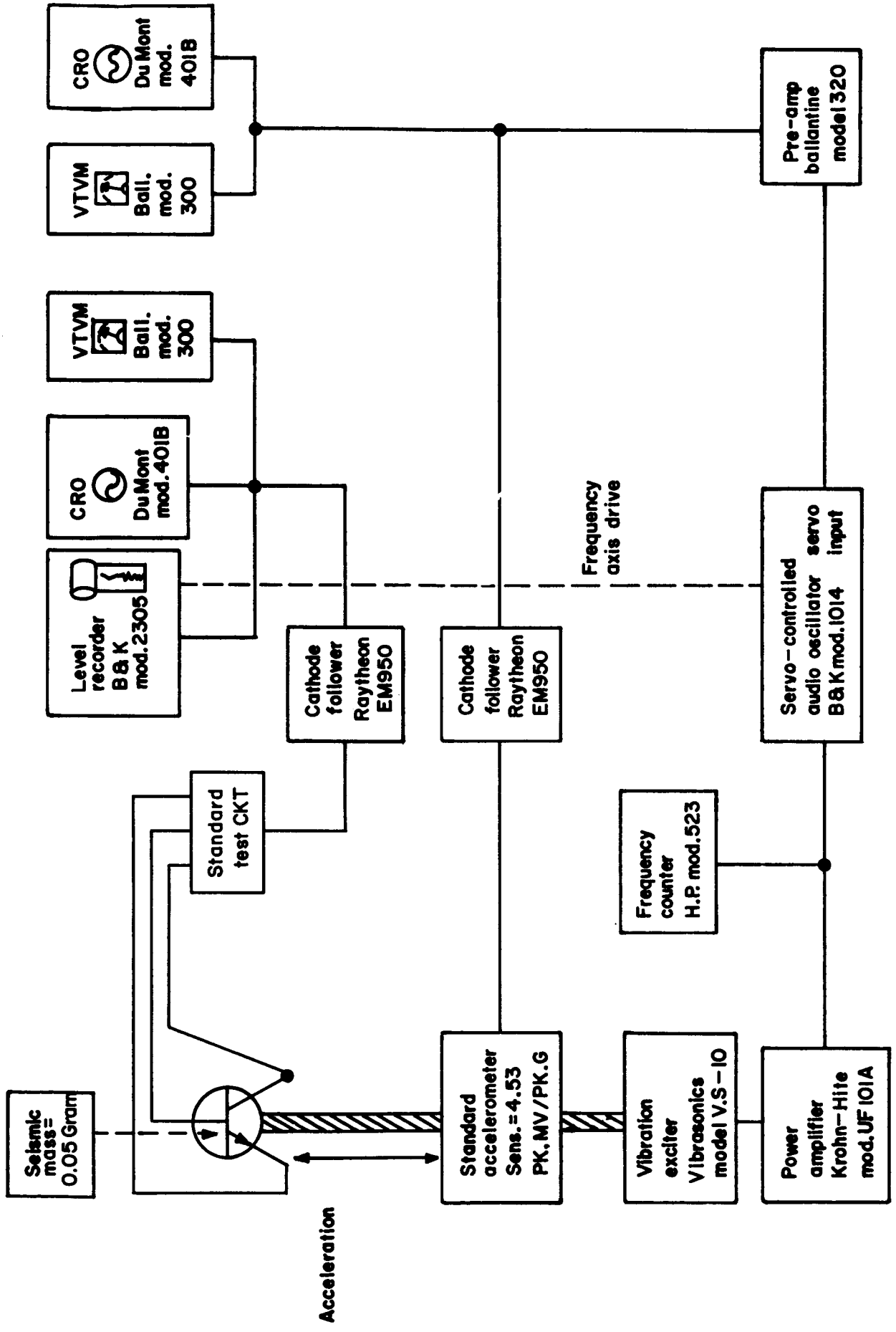


Figure 31 Schematic Representation of Accelerometer Calibration System

4.2.2 Sensitivity, Linearity, and Frequency Response

Sensitivity of different sensors fabricated under this contract has varied from essentially zero to greater than 100 pk mV/pk G, but in all cases where sensitivity was below 30 pkmV/pk G, evidence of overstressing could be detected in the degraded transistor characteristics. Individual devices usually show an initial sensitivity loss of 5-10 percent during the first day, and then a slow increase of 10-20 percent during the next few weeks. No attempt was made to hasten stabilization by thermal cycling or other means commonly employed for such purposes with most other transducer types. Three weeks to a month after fabrication the drifts become random within a ±5 percent band, and further gross changes should not be expected unless overstressing occurs. The sensors should not be dropped, the exposed diaphragm must not be touched; and the acceleration level during tests must not exceed 20 G at low frequencies or 1 G at the resonance frequency.

The linearity determined by 0.1G, 1G, and 10G vibration calibration at 100 Hz is within the ±5 percent over-all test equipment error band. More precise pressure measurements of the basic piezotransistor imply that linearity is actually better than 2 percent, but we presently lack means of verification by acceleration input.

Piezotransistor acceleration sensors in the fixture of Fig. 30 have shown a remarkable similarity in frequency response, Fig. 32 being a representative curve. The irregularities in the neighborhood of 400 Hz are caused by clearly-seen resonances of the leadwire stubs and should not affect a properly packaged accelerometer. The resonance frequency of all devices so tested has been 16 kHz±10 percent, and is undoubtedly influenced by the relatively large holder, which was designed primarily for testing convenience rather than best high frequency characteristics. Output at resonance is approximately 38 dB above the mid-band value.

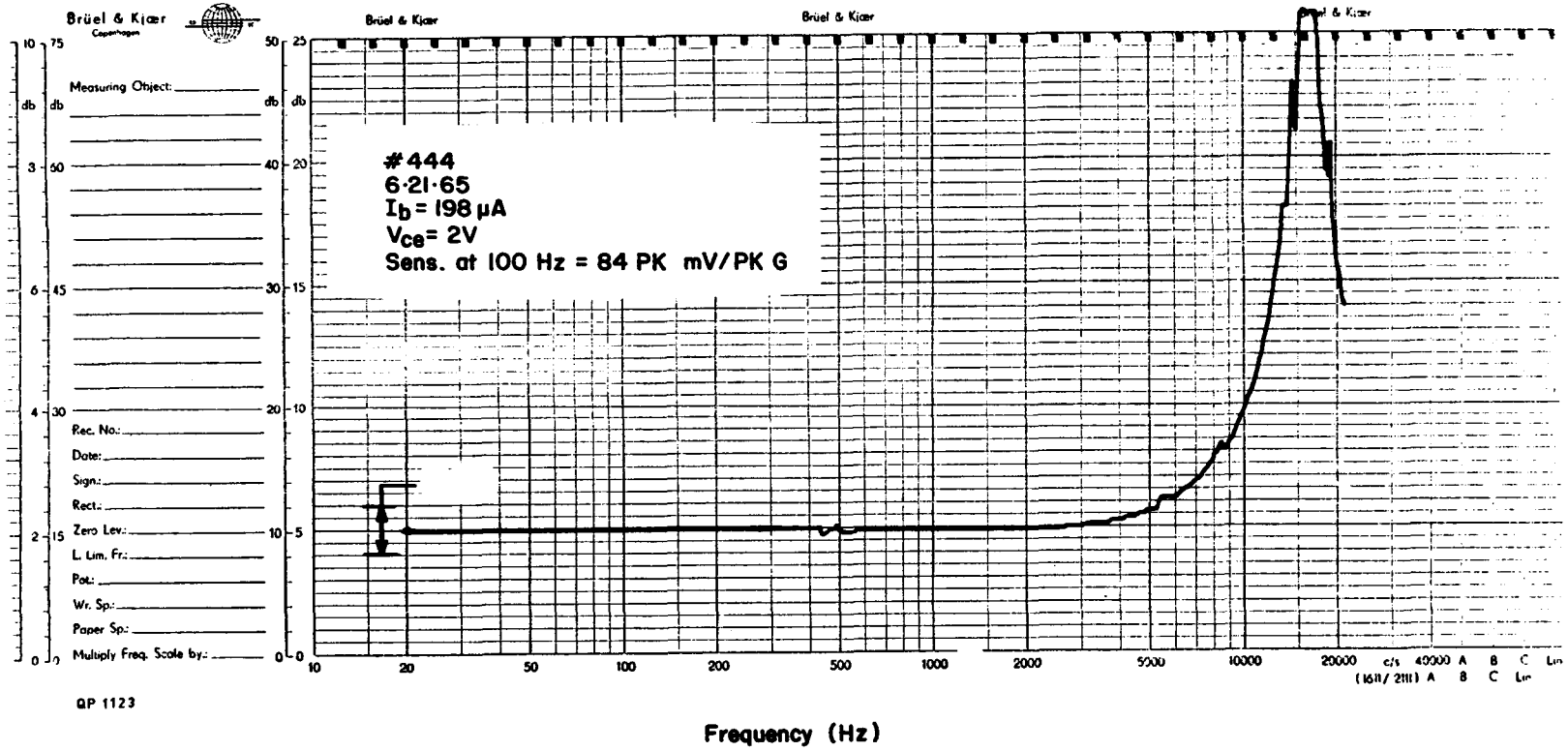


Figure 32 Typical Piezotransistor Acceleration Sensor Frequency Response

4.2.3 Behavior with Temperature

Using flat diaphragms on both the basic element and the upper mass support, the thermal characteristics of the acceleration sensor are essentially those of the basic element, as previously described. Dishing the upper diaphragm to a one-half inch radius of curvature, however, in combination with a flat diaphragmed piezotransistor, resulted in an acceleration sensor with a temperature coefficient of similar magnitude but opposite sign, demonstrating the feasibility of temperature compensation by this simple means. Because of the time spent in solution of more basic problems, temperature compensation was not intensively studied, but feasibility was shown and this is clearly a fruitful area for future work.

5. PACKAGED PIEZOTRANSISTOR ACCELEROMETER

5.1 Design Objectives

For practical use, the previously described acceleration sensor must be protected by a sealed enclosure, primarily to prevent humidity damage and excessive sensitivity to acoustic noise. The enclosure should be corrosion resistant, light in weight, and should protect against damage from careless handling. It should attenuate test specimen stresses and all other spurious perturbations, so that the instrument responds primarily to axial acceleration. A means must be provided for mounting to a test specimen. Although the use of adhesives for this purpose is increasing, a threaded stud is still preferred, particularly when the transducer is novel and will be exposed to frequent calibration. Because of the heavy ground loops and inter-channel interferences encountered in many field installations the mounting means should provide electrical insulation between specimen and sensor, but not at the expense of tight mechanical coupling. A connector should be provided, so that replaceable cables may be used, since they are often damaged during installation in tight spaces; furthermore, it is difficult to properly seal an integral cable entry.

The housing resulting from these considerations, shown in sectional form in Fig. 33, is machined from two pieces of 303 stainless steel. The air space surrounding the sensor provides mechanical decoupling from the case. Rigid epoxy potting compound insulates the mounting surface from the sensor, and also provides sealing and support to the integral cable. Although the main transmission path from mounting surface to sensor is through epoxy, the large area and thin section of this material minimize compliance, so that the effect on accelerometer resonance frequency should be negligible.

We were unable to find a connector suitable for such a small accelerometer. An extensive survey revealed that the smallest connector sets available would be many times larger and heavier than the entire sensor,

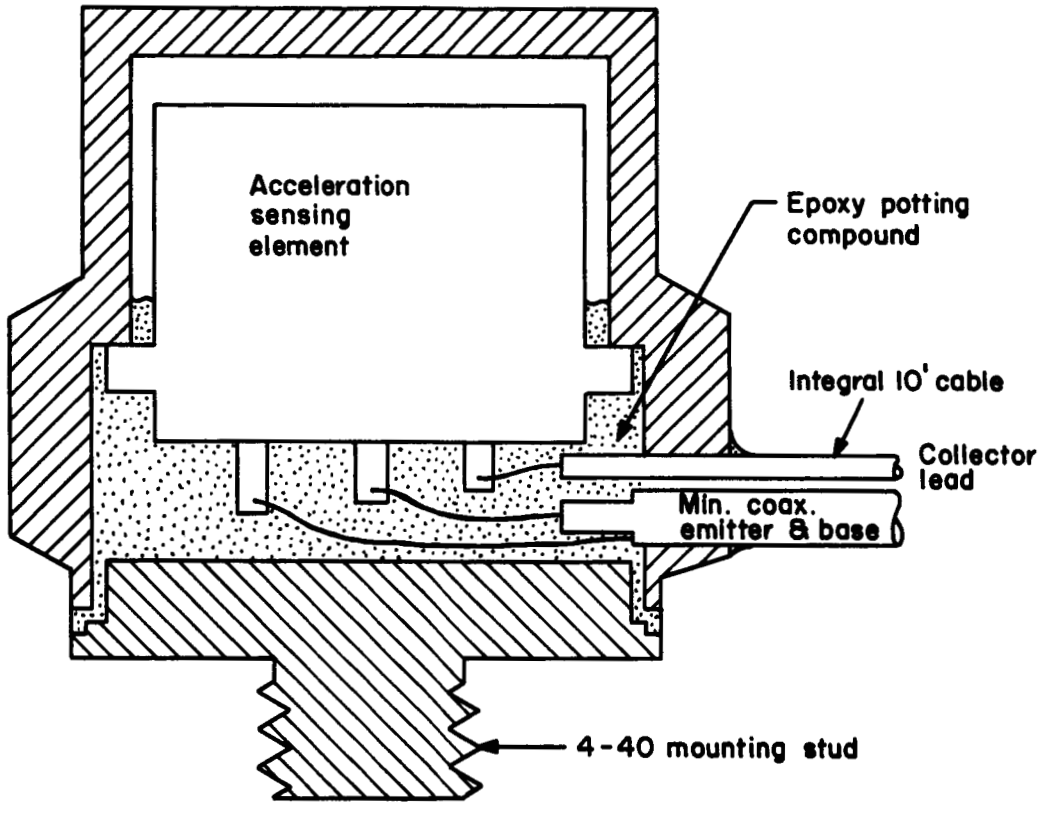


Figure 33 Sectional View of Packaged Piezotransistor Accelerometer

so the decision was reluctantly made to use an integral cable. The base lead is shielded by the emitter in 0.045 in. diameter coaxial cable; the collector lead, which is indifferent to electromagnetic interference, is an insulated, stranded wire of the type normally used to connect phonograph cartridges. Figure 34 shows a finished accelerometer, which is 0.330 in. high by 5/16 hex, and weighs 2.5 grams.

5.2 Fabrication

In common with the basic piezotransistor and the acceleration sensing element, the accelerometer assembly procedure is simple in principle but fraught with difficulty in practice. Four samples were prepared substantially as described below.

The flushing holes in the header of a previously checked acceleration sensor are plugged with crystalline wax, and the sensor flange is bonded to the shoulder in the upper housing. A thixotropic epoxy is used in this step to avoid the possibility of flow into the air space. After curing, a cable with properly prepared ends is fed through the hole in the housing, dressed close to the header, and soldered or welded to the transistor lead stubs. The cable entry is caulked with thixotropic epoxy and cured. An easy-flowing epoxy resin is then poured into the cavity to within 1/32 in. of the rim, the same material is brushed in a thin coat on the upper surfaces of the mounting base. After both parts are cured, a large drop of epoxy is placed in the cavity and the two parts of the housing are joined. The excess epoxy is wiped as it extrudes around the periphery, and a final curring completes the assembly.

Unfortunately, all four of the accelerometers so packaged deteriorated during the final assembly and now show characteristics typical of overstressing. Solder was used for internal connections in the first three accelerometers, the last was spot welded, but all show substantially the same type of degradation. While discouraging, the results are not surprising,

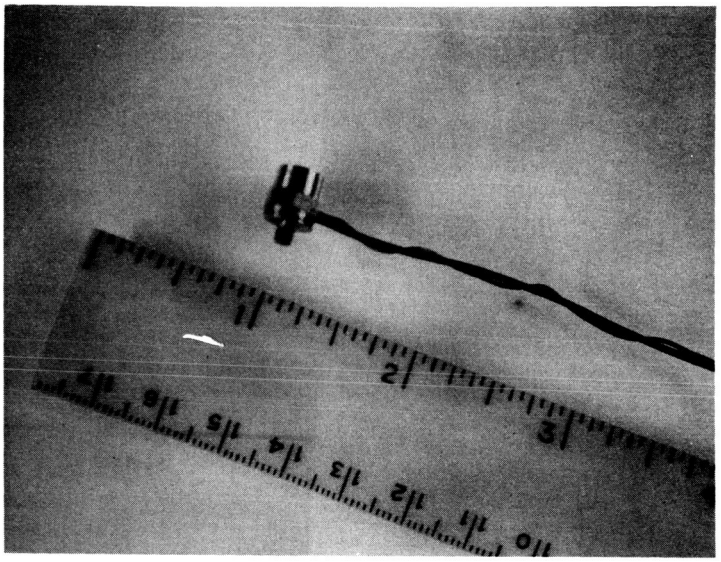


Figure 34 Photograph of Finished Accelerometer

for we encountered and solved similar problems during each preceeding phase. Time, however, had run out during final assembly of these four devices, so that processing corrections were not possible under the present contract.

6. UNIAXIALLY STRESSED JUNCTIONS

In the course of the efforts made by us and others to better understand and thus, finally, to better control the ASE in useful applications, the contribution of uniaxial compression to the effect was investigated theoretically and experimentally. Our recent experimental work shows that there exists in fact a uniaxial ASE of considerable magnitude which seems to be basically different in physical origin than the ASE under point stress.

As part of our effort to exploit the ASE we have made the first steps to assess the device potentialities under uniaxial conditions. The primary difficulty to be overcome was the development of a technique to permit safe application of pre-stress close to the fracture point of the material. Device structure was designed around samples, about $0.5 \times 0.5 \times 2.0$ mm, containing a junction about in the middle of the long axis originally intended for the study of the effect per se. The schematic representation in Fig. 35 shows the experimental details of our initial design and should require little comment. Brass electrodes were used as pressure contacts. An important role is played by the so-called "Bellville" washer which is designed to retain essentially constant stiffness over a large range of dimensional changes, thus facilitating the device assembly at the expense of some stress sensitivity.

The initial attempts to assemble devices in this structure revealed difficulties in alignment and retaining of integrity of the samples. The first devices completely assembled showed evidence of damage to the semiconductor and thus do not reflect the inherent device characteristics. Further efforts will be required to eliminate these difficulties. Continued work in this direction appears to be worthwhile to establish the device potential of this new form of the ASE.

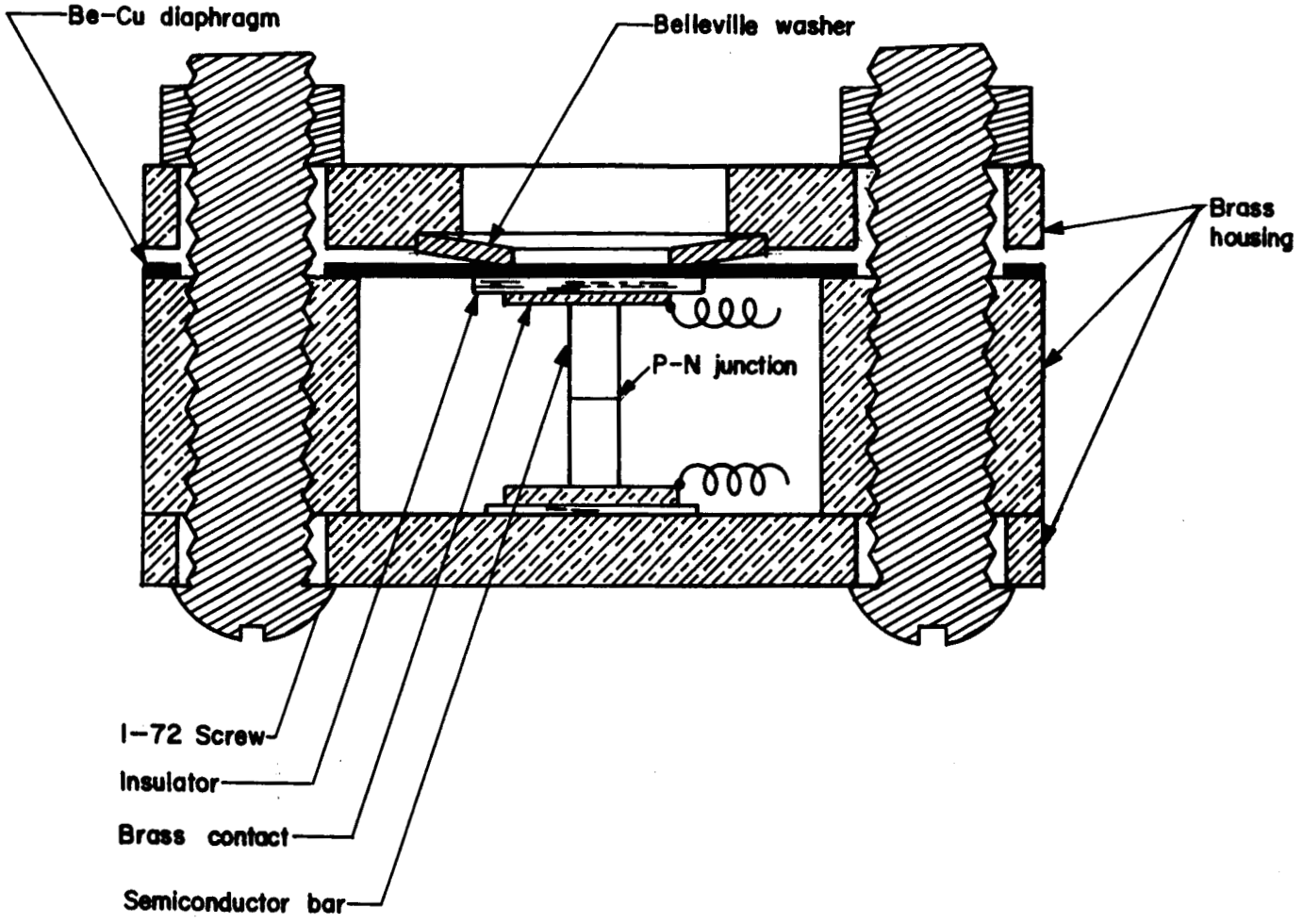


Figure 35 Uniaxially Stressed P-N Junction Device

7. SUMMARY AND RECOMMENDATIONS

Procedures developed during this program for fabrication of the basic element and the acceleration sensor will allow future preparation of those devices with good yields, paving the way for a new generation of transducers. Considerable insight was gained into their behavior, into failure modes and probable causes, into their potentialities and limitations. We identified the major cause of temperature drift and showed the feasibility of compensation.

Although the work with integrated bridge circuits was successful, it proved to be not particularly pertinent to the present program, inasmuch as the thermal drift in transistor characteristics per se is a minor contributor to the over-all thermal behavior of practical devices and such compensation was the primary reason for this phase. Perhaps the major significance of the integrated circuit work was the successful assembly of an acceleration sensor based on an extensively modified monolithic chip, in which the finished device characteristics compared favorably with those of simple piezotransistor sensors. The relevance to future advances in data acquisition is obvious, and some form of direct digital output from a minute integrated accelerometer should be pursued by further research and development.

After many initial failures, five good acceleration sensors were prepared from piezotransistors and one from an integrated bridge circuit. Although success occurred late in the program it is noteworthy that the last six devices were assembled without intervening failures. The inability to package those sensors and the ruin of four in attempts to do so was disappointing; however, we are confident that no basic barriers exist and we recomment pursuit of this goal in the future.

The work with uniaxially stressed junctions was purely exploratory, and our experience with point-stressed devices leads us to believe that exploitation of the uniaxial effect in practical transducers must be preceeded by

a great deal of research in order to understand its peculiarities and to develop familiarity with processing and handling requirements. Nevertheless, this should be started, for theoretical considerations indicate that such devices should possess greater uniformity and stability than those based on anisotropic stress.

This program has had considerable impact on the views of the investigators. During the past year we have gained further confidence in the ultimate device potential of the ASE; at the same time we are more fully aware of the pitfalls, and we realize that success will require a large amount of work for solution of the ancilliary problems that arise with each step forward.

REFERENCES

1. W. Rindner, J. Appl. Phys. 33, 2479 (1962).
2. W. Rindner and I. Braun, J. Appl. Phys. 34, 1958 (1963).
3. W. Bernard, W. Rindner, and H. Roth, J. Appl. Phys. 35, 1860 (1964).
4. J. J. Wortman, J. R. Hauser, and R. M. Burger, J. Appl. Phys. 35, 2122 (1964).
5. R. Edwards, Proc. IEEE-ED11, 286 (1964).